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Methods

Ge/Si core/shell nanowire synthesis. Ge/Si nanowires were synthesized using the Au-nanocluster-catalyzed methodology described previously[1-3]. 10 nm diameter gold nanoparticles (Ted Pella) were dispersed on the oxide surface of silicon/SiO_2 substrate (600 nm oxide) and placed in the central region of a quartz tube reactor system. The Ge-core is synthesized at 270 ^oC and 450 torr, with 30 sccm germane (GeH_4, 10% in H_2) and 200 sccm H_2 as the Ge reactant and carrier gas, respectively. The growth was carried out for 40 min to yield NWs with >35 μm length. Without opening the growth system, the epitaxial Si shell was then grown at 460 ^oC and 5 torr for 2 min, using 5 sccm pure silane (SiH_4) as the Si source. The growth system was pumped down to 3 mtorr and purged with H_2 for 5 min between the growth of Ge-core and Si-shell.

ALD growth of oxide dielectric shells. The device substrate with Ge/Si NWs and source/drain contacts was placed in the ALD chamber (Savannah-100, Cambridge NanoTech) heated to 200 ^oC. Trimethyl aluminum [$Al(CH_3)_3$, TMA], tetrakis(dimethylamino)zirconium {$Zr[N(CH_3)_2]_4$} and water were used as precursors[4-5]. Each Al_2O_3 deposition cycle consisted of 0.015 s water vapor pulse, 8 s N_2 purge, 0.015 s TMA pulse and 8 s N_2 purge. Each ZrO_2 deposition cycle consisted of 0.015 s water vapor pulse, 10 s N_2 purge, 0.25 s Zr-precursor pulse and 15 s N_2 purge. To form the charge-trapping dielectric structure shown in Fig. 1b, a deposition sequence of 25 cycles Al_2O_3, 55 cycles ZrO_2 and 55 cycles Al_2O_3 was used.

Contact Printing of NWs. Ge/Si NWs were transferred from growth substrates to device substrates by a shear printing process where shear force determines the density and alignment of NWs[6]. First, oxygen plasma treated (80 W, 1 min) device substrates (600 nm SiO_2/Si) were patterned by photolithography (Shipley S1805 diluted 50 % in Thinner-P, MicroChem) to define a region where NWs will be deposited. The dimension of the region was typically ~1 cm (width) by ~1 mm (length). Second, the patterned device substrate was mounted onto a fixed stage whose movement can be controlled by a micromanipulator. Approximately 50 μL of mineral oil (heavy mineral oil, Sigma-Aldrich) was drop-casted onto the device substrate to serve as a lubricant. Third, the NW growth substrate (~1 cm by 2 cm) was brought into contact with the device substrate (NWs facing the device substrate) and a pressure of ~3.43 N/cm^2 was applied while the device substrate was slid with a constant velocity of ~5 mm/min. These procedures produced an average printing density of ~1 Ge/Si NW per micron.

Fabrication of nanowire logic tile. The large-area Ge/Si NW array was first patterned into proper dimensions for device fabrication, using an inductively coupled plasma reactive ion etching (ICP-RIE, Surface Technology Systems). SF_6 was used as etchant and electron beam lithography (EBL, with PMMA 950-C2, Microchem) was used to mask regions for devices. Dark-field optical microscopy was used to register the positions of individual NWs, and then source/drain contacts were defined by EBL followed by wet etching in 1:7 buffered oxide etchant (BOE, Transene) for 5 seconds and thermal evaporation of 70 nm Ni. The dielectric layers were deposited by ALD followed by EBL and metallization to define top-gate metal lines (Cr/Au, 2/70 nm respectively). The dielectric over the outer metal was etched with 1:7 BOE for 15 s to allow electrical access to the devices. Finally, EBL and metal evaporation were used to connect source/drain/gate electrodes to the outer metal pads.

Programming and characterization of nanowire logic circuits. Device chips were mounted in a probe station (Model 12561B, Cascade Microtech) with the back-plane grounded. A custom-designed 96-pin probe-card (Accuprobe) equipped with BNC interface was used to electrically

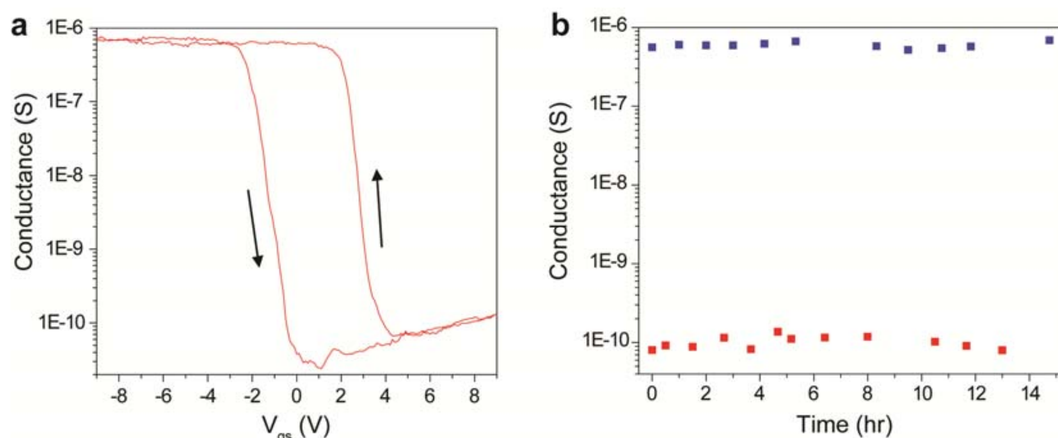
access the devices in the array. Measurements were made with a computer-controlled analog I/O system (PXI-6723, 3x PXIe-6124 in a PXIe-1065 chassis, National Instruments) that provided 32-channel analog-voltage generation and 12-channel analog-voltage recording. Each analog-voltage recording channel has >100 GΩ input resistance which is over 10^4 larger than the resistance of NWFETs (≤1 MΩ) and passive load resistors (≤10 MΩ) used in the circuits. The 2-NW coupled circuit, full-adder, full-subtractor, D-latch and MUX/DEMUX shown in Figs. 2a, 3c, 4a, 4d, and Supplementary Fig. S6, respectively, were programmed following the $V/3$ rule[7] (Supplementary Fig. S5), with a programming voltage, V, of -6 V. The detailed programming procedure is described as follow. First, all NWFET nodes in both blocks were set to inactive by applying (1) $-V$ to all top-gates in block-1; (2) 0 to the source/drain contacts of the NWs in block-1; and (3) V to the source/drain contacts of the NWs in block-2. Second, the active node pattern (green dots in Figs. 2a, 3c, 4a, 4d, and Supplementary Fig. S6) in block-1 was programmed by applying (1) V and $V/3$ to the selected and non-selected top-gates in block-1, respectively; (2) 0 and $2V/3$ to the source/drain contacts of the selected and non-selected NWs in block-1, respectively; and (3) $V/3$ to the source/drain contacts of NWs in block-2. This allowed the selected gate nodes to be biased at V, while all the other nodes were biased at $\pm V/3$. Third, the active node pattern in block-2 was programmed in the similar fashion. For the node programming described above, programming voltages were applied for 2 s in each step. The D-latch shown in Fig. 4d was programmed similarly, with the feedback from output Q to the block-1 top-gate disconnected during programming, and re-connected for the measurement. Measurements were made using source voltages of 3, 2.5 and 2.2 V for the full-adder (Fig. 3c), D-latch (Fig. 4d) and MUX/DEMUX (Supplementary Fig. S6) circuits, respectively. These source voltage values allowed input/output voltage matching. The input gate voltages were 0 V for logic "0" and 3 – 3.6 V for logic "1" in these cases. For the full-subtractor, the source voltage was 1.5 V for block-1 and 0.1 V for block-2, and the input gate voltages were 0 V for logic “0” and 2.5 V for logic “1”. The smaller source voltages were used initially in studies of both full-adder and full-subtractor to demonstrate all logic combinations, while input/output voltage matching, which required larger source voltages, was the focus of later measurements on the full-adder, MUX/DEMUX and D-latch.

To record the voltage outputs from the circuits, we connected external resistors (≤10 MΩ metal film resistors with ±1% tolerance, Vishay Dale) to the drain of individual NW devices in the NW logic tile and monitored output voltage at the drain electrode. The value of the external resistors was chosen to be at least one order of magnitude larger than the ‘on’ state resistance of active nodes. The passive resistor loads used in our circuit prevented us from achieving full-swing operation, although future integration of complementary NWFET loads[8] can minimize this effect. Simplified circuit schemes excluding resistor connections were presented in Figs. 2, 3, 4 and Supplementary Figs. S5 and S6. The 2-NW coupled circuit (Fig. 2a) was measured at 0.3 Hz input signal on G1; the full-adder (Fig. 3e) and full-subtractor (Fig. 4b) were measured at 1 Hz input gate signals; the MUX/DEMUX (Supplementary Fig. S6b, e) were measured at 0.5 Hz input signals; and the D-latch (Fig. 4e, f) was measured at ~0.06 Hz Data (D) and Clock (E) signals.

Comparison of nanowire logic tile and top-down CMOS logic

First, the effective area per transistor without overhead in the un-optimized NW array demonstrated in this work is ~1.9 μm^2, which is larger than that of 0.09 μm^2 in the logic gates of the present 32-nm CMOS generation[9]. The projected area per NW transistor may be reduced by

up to several orders of magnitude in the future using dense packed NWs, which have been demonstrated by Langmuir-Blodgett assembly[10], and based on the reported scaling of charge-trapping devices[11]. Second, the estimated power consumption of each NW logic gate is ~0.9 μW based on V_{DD} of ~3 V and on-state current of ~0.3 μA. This is larger than the 10-100 nW per gate consumed in 32-nm CMOS. However, the use of complementary p-type/n-type NW devices[8] would eliminate static power dissipation and could reduce substantially power consumption per NW logic gate. Third, the prototype demonstrated in this work was developed to demonstrate correct static operation and was not optimized for maximum operating speed. Simulations carried using both measured NW properties and projected improved circuit designs[12,13] suggest that a circuit speed on the order of 100 MHz would be achievable, which is comparable to clock speeds required in real-time, low-power microcontrollers[14] but less than the 5 GHz achievable in conventional CMOS[9] for high-performance computing. It is noteworthy that the speed of the nanoprocessor is not limited by the intrinsic characteristics of NWs, as previous studies of Ge/Si NWFETs with 40 nm channel length has shown potential for 2 THz switching[15], which defines an upper limit for Ge/Si NWFET-based logic operations.



Supplementary Figure S1 | Stability of charge-trapping states in nonvolatile NWFET. To probe the intrinsic stability of the charge-trapping states, measurements were made in a vacuum chamber at ~0.5 mtorr. The test device has a similar multi-gate geometry as shown in Fig. 1c. Before the tests all gate nodes were set to inactive by applying +9 V V_{gs} for 10 s. Then one top-gate was used for the test while all other top-gates were floating. The back-plane of the device chip was grounded throughout the test. **a**, Semi-logarithmic plot of the conductance vs. V_{gs} curve measured at 0.5 V V_{ds}. The arrows represent the direction of sweep/hysteresis. The rise of conductance at large positive V_{gs} is due to ambipolar conduction[3]. **b**, Conductance vs. time for active (red) and inactive (blue) states of the same device as in **a**. Active and inactive states were programmed by applying (-9 V, 10 s) and (+9 V, 10 s) pulses to the top-gate, respectively. The conductance levels were measured at 0.5 V V_{ds} and 1 V V_{gs}. The source, drain and top-gate electrodes were floating between measurements. No sign of state degradation was observed for either active or inactive settings throughout the period of test (13 hr for active state and 15 hr for inactive state). We note that the stability of our NWFET device is at least comparable to that of a planar charge-trapping memory device with similar charge-trapping dielectric structure[16]. This planar structure showed ~10% charge leakage in the same period of time and was reported[16] to have a projected retention time of >10 years.

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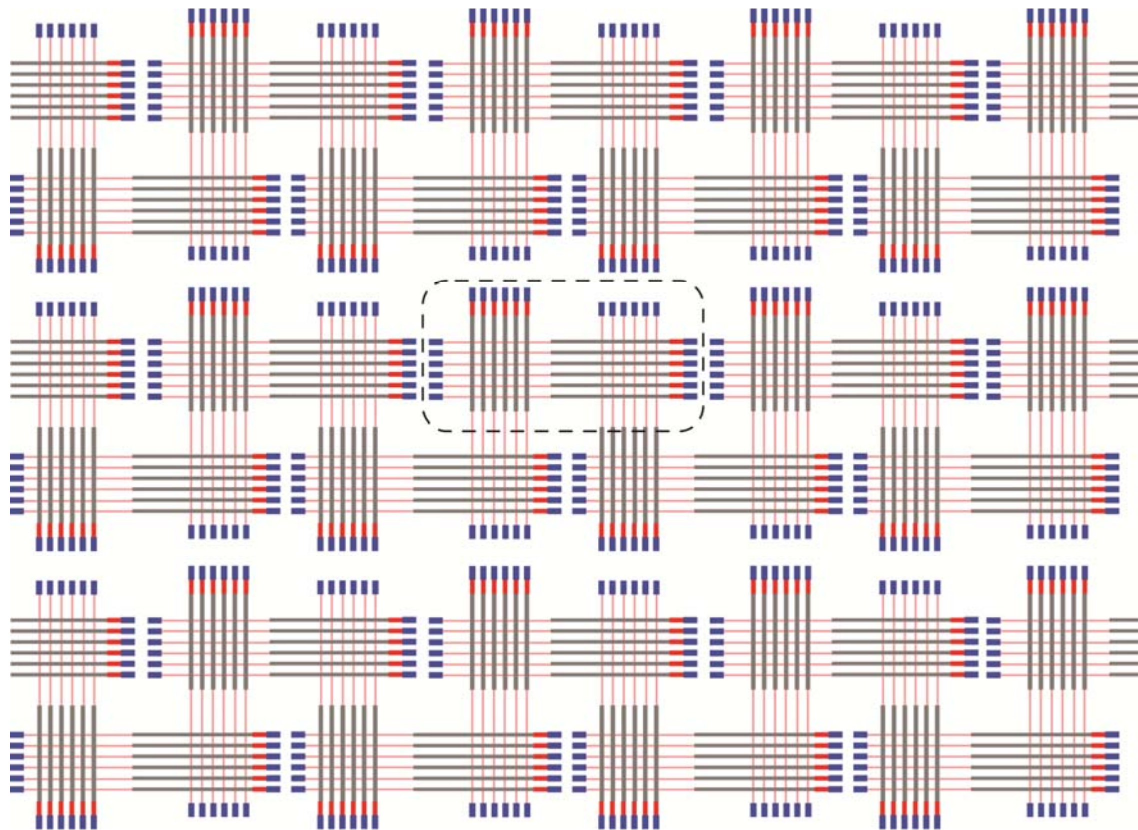
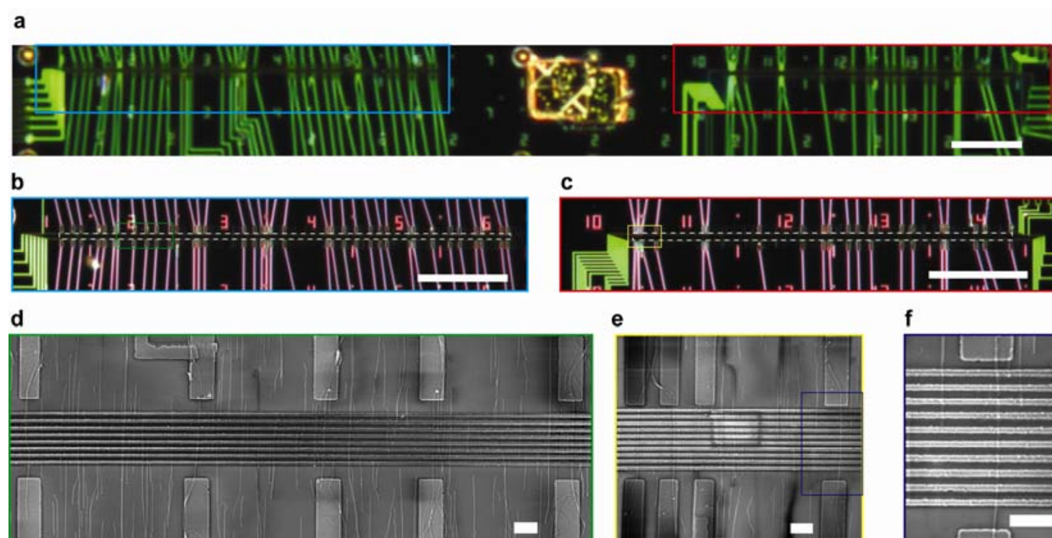
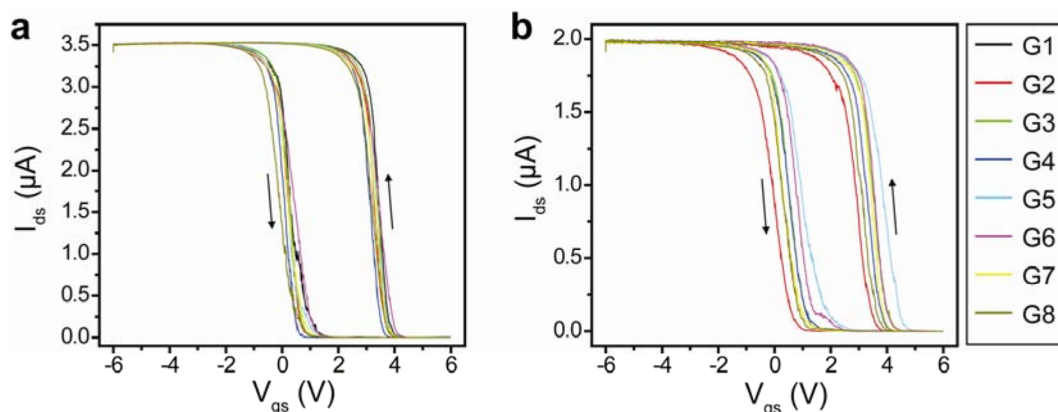


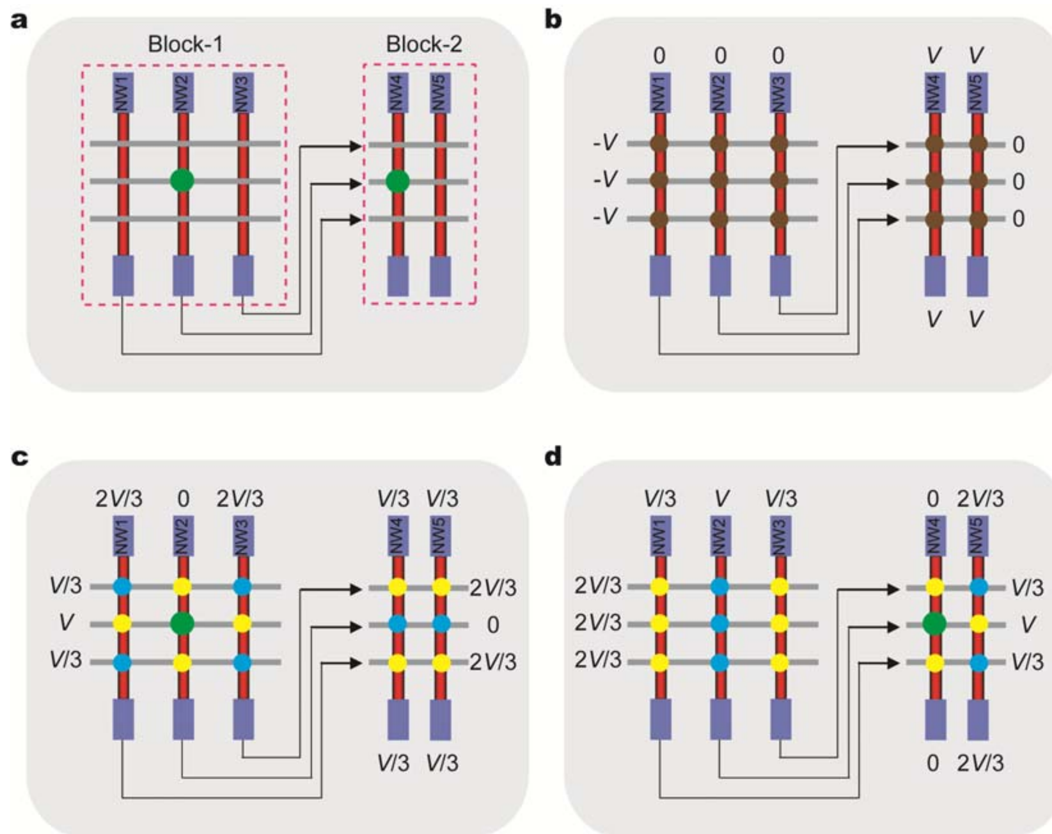
Supplementary Figure S2 | Nanoprocessor architecture based on the NW logic tile. The unit tile (dashed box) corresponds to the schematic shown in Fig. 2b, and is composed of two NW arrays, block-1 (left) and block-2 (right). Each block contains charge-trapping NWs (pink), metal gate electrodes (grey), load devices (red) and lithographic-scale electrodes (blue) integrated for I/O. Note that the NWs and metal gates in block-1 are rotated 90° with respect to the schematic shown in Fig. 2b. The unit tiles are cascaded by feeding the outputs of one tile to the inputs of the next tile, forming a feed-forward logic architecture capable of combinational logic functions. Sequential logic functions such as latches can be implemented by integrating control gates[17] or switchable diodes[18] in the architecture to allow for programming and feedback.



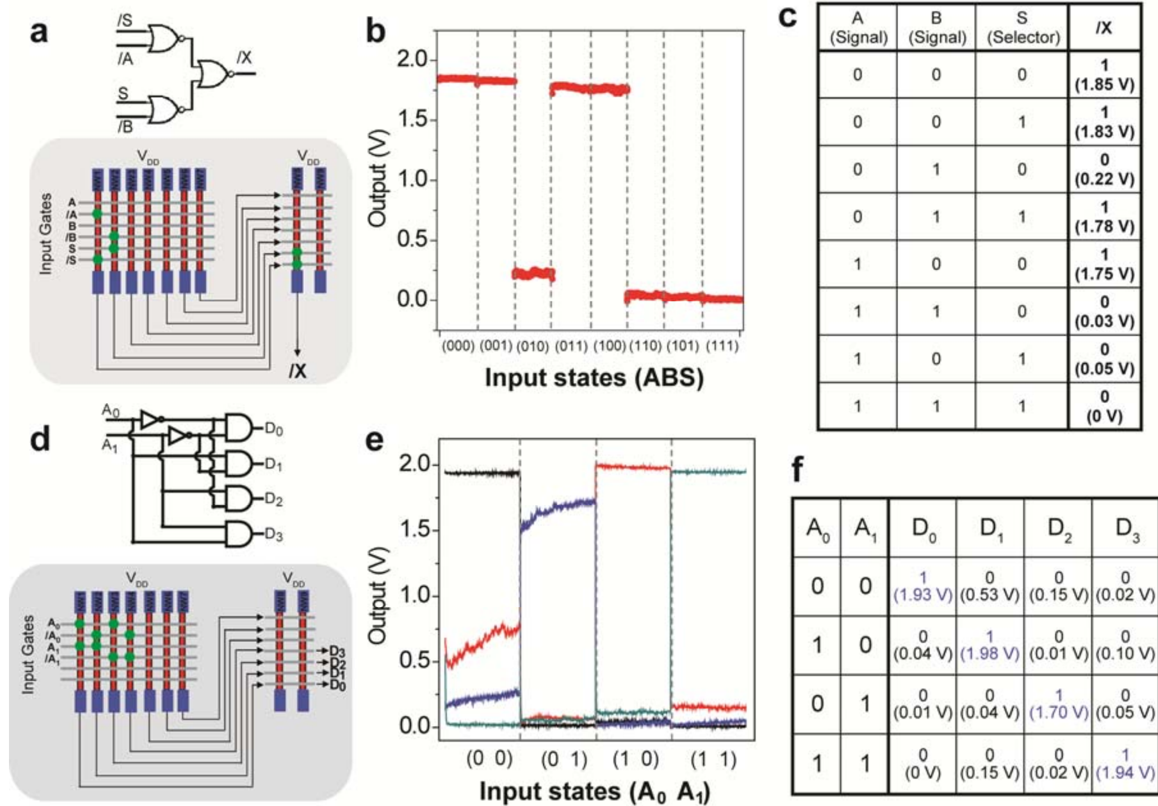
Supplementary Figure S3 | NW logic tile. **a**, Dark-field optical microscope image of the two-block NW logic tile. The cyan (left) and red (right) open rectangles outline block-1 and block-2, respectively. Scale bar, 40 μm. **b,** Dark-field optical image of the block-1 from the region defined by the cyan rectangle in **a**. The white dashed box at the central region of the image outlines the region containing NWFET devices. Scale bar, 40 μm. **c**, Dark-field image of the block-2 from the region defined by the red rectangle in **a**. The white dashed box at the central region of the image outlines the region containing NWFET devices. The total area of the regions defined by the white dashed boxes in **b** and **c** is ~960 μm^2. Scale bar, 40 μm. **d**, SEM image of the region defined by the green rectangle in **b**. Scale bar, 1 μm. **e**, SEM image of the region defined by the yellow rectangle in **c**. Scale bar, 1 μm. **f**, SEM image of the region defined by the blue rectangle in **e**, showing a single-NW device with 10 top-gates. Scale bar, 1 μm. The optical images were taken in dark-field mode (BX51, Olympus) with 5x (**a**) and 20x (**b**, **c**) objective lenses. SEM images were taken in a field-emission SEM (Ultra55, Zeiss) with 2 kV acceleration voltage and in-lens detector.



Supplementary Figure S4 | Characterization of NWFETs in the logic tile structure. **a-b**, Typical I_{ds} vs. V_{gs} data of NW devices in **a**, block-1 (left array) and **b**, block-2 (right array) as shown schematically in Fig. 3c. The devices were biased at 0.5 V. The measurement was taken by scanning the V_{gs} on one gate line from 6 V to -6 V and then back to 6 V, while keeping the other gate voltages at 0 V. Prior to the measurement all the gate lines were biased at 6 V for 5 s to reset all of the NWFET nodes into inactive state. The arrows mark the direction of the hysteresis. The different colored curves represent recording from different gate lines (G1 ~ G8).



Supplementary Figure S5 | Schematic of active node pattern programming using *V*/3 rule. a, Schematic of the circuit and the target active node pattern (green dots). The illustration shows three NWs (NW1-NW3) in block-1 (left pink dashed box) and two NWs (NW4-NW5) in block-2 (right pink dashed box), both with three top-gates (grey). The two blocks are connected by external wiring (black lines with arrows) before programming. **b-d**, Step-by-step programming of the active node pattern shown in **a** without affecting the state of the other nodes. For each step the voltages applied to the source/drain electrodes of the NWs (V_{NW}) and the top-gates (V_{TG}) are marked beside their corresponding terminals. Typical value of the programming voltage, V, is -6 V. The voltage drop across the charge-trapping dielectric, V_{gs}, is defined as V_{TG} - V_{NW}, and is presented by colored dots as explained in details below. **b**, All nodes are first set to inactive by setting V_{gs} to $-V$ (brown dots). **c**, Active node on NW2 in block-1 is programmed, by setting V_{gs} to V (green dot) for the target node, and $V/3$ (yellow dots) or $-V/3$ (cyan dots) for all other nodes. **d**, Active node on NW4 in block-2 is programmed in similar fashion as **c**. Note that in **c-d**, V_{gs} is at V only for the target node, and is at $\pm V/3$ for all other nodes in both blocks. The successful implementation of various logic circuits (Figs. 2-4, S6) demonstrates that the $\pm V/3$ V_{gs} does not disturb the charge-trapping states of these nodes, and thus confirms the validity of this programming approach. See above Methods section “Programming and characterization of nanowire logic circuits” for additional details.



A (Signal)	B (Signal)	S (Selector)	/X
0	0	0	1 (1.85 V)
0	0	1	1 (1.83 V)
0	1	0	0 (0.22 V)
0	1	1	1 (1.78 V)
1	0	0	1 (1.75 V)
1	1	0	0 (0.03 V)
1	0	1	0 (0.05 V)
1	1	1	0 (0 V)

A_0	A_1	D_0	D_1	D_2	D_3
0	0	1 (1.93 V)	0 (0.53 V)	0 (0.15 V)	0 (0.02 V)
1	0	0 (0.04 V)	1 (1.98 V)	0 (0.01 V)	0 (0.10 V)
0	1	0 (0.01 V)	0 (0.04 V)	1 (1.70 V)	0 (0.05 V)
1	1	0 (0 V)	0 (0.15 V)	0 (0.02 V)	1 (1.94 V)

Supplementary Figure S6 | MUX and DEMUX circuits implemented in the NW logic tile architecture. a-c, Characterization of a 2-to-1 MUX. **a**, Schematic of logic (upper) and circuit implementation (lower) of MUX. The circuit involves 2 NWs in block-1, 1 NW in block-2 and 6 input gates (*A*, *B*, *S*, and complements). The *S* signal selects the output *X* between *A* and *B*. Note that in this demonstration the complementary signal (*/X*) is generated, which can be easily translated to *X* by using an additional NWFET as an inverter. **b**, Voltage output (*/X*) at 8 input states. The circuit was realized using the same NW logic tile structure as shown in Fig. 3c. The levels of logic "0" and "1" are well separated: 0 – 0.22 and 1.75 – 1.85 V, respectively. **c**, Truth table of the MUX. The measured voltage outputs are summarized in the brackets. **d-f**, Characterization of a 2-to-4 DEMUX. **d**, Schematic of logic (upper) and circuit implementation (lower) of the DEMUX. The circuit uses 4 NWs in block-1 and 4 gates (A_0, A_1 and their complementary inputs). The 4 outputs (D_0 – D_3) are addressed by combinations of (A_0, A_1). **e**, Voltage output of D_0 (black), D_1 (red), D_2 (blue) and D_3 (cyan) at different (A_0, A_1) input states. The level of logic "0" is 0 – 0.7 V and logic "1" is 1.5 – 2 V. **f**, Truth table of the DEMUX. The measured voltage outputs are summarized in brackets. The blue color marks the line that is selected at each input combination.

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