Diameter-dependent dopant location in silicon and germanium nanowires

Ping Xie[a], Yongjie Hu[a], Ying Fang[b], Jinlin Huang[a], and Charles M. Lieber[a,c,1]

[a]Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138; [b]National Center for Nanoscience and Technology, Beijing 100190, China; and [c]School of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138

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We report studies defining the diameter-dependent location of electrically active dopants in silicon (Si) and germanium (Ge) nanowires (NWs) prepared by nanocluster catalyzed vapor-liquid-solid (VLS) growth without measurable competing homogeneous decomposition and surface overcoating. The location of active dopants was assessed from electrical transport measurements before and after removal of controlled thicknesses of material from NW surfaces by low-temperature chemical oxidation and etching. These measurements show a well-defined transition from bulk-like to surface doping as the diameter is decreased <22–25 nm for *n*- and *p*-type Si NWs, although the surface dopant concentration is also enriched in the larger diameter Si NWs. Similar diameter-dependent results were also observed for *n*-type Ge NWs, suggesting that surface dopant segregation may be general for small diameter NWs synthesized by the VLS approach. Natural surface doping of small diameter semiconductor NWs is distinct from many top-down fabricated NWs, explains enhanced transport properties of these NWs and could yield robust properties in ultrasmall devices often dominated by random dopant fluctuations.

nanoelectronics | surface doping | surface segregation | vapor-liquid-solid growth

The incorporation of electrically active dopants in semiconductor materials has been central to development of electronic and optoelectronic devices (1, 2). Dopants can be introduced in well-defined concentrations during the growth of bulk crystal (1), yet in synthesized nanoscale structures, such as nanoparticles and NWs, the incorporation of dopants during growth may be affected by kinetic and thermodynamic factors associated with finite size (3–9). Difficulties in incorporating dopants into nanoparticles have been attributed to surface energetics within the context of the kinetics for colloidal growth (3, 4) and thermodynamic factors during high-temperature growth (5). In the case of synthesized semiconductor nanowires, there is considerable evidence from electrical transport measurements that active dopants can be incorporated during growth (6–9). However, details of the distribution of dopants within these nanostructures and size-dependent doping, which are critical to the fundamental understanding of their behavior, modeling, and applications of nanoelectronic devices based on NWs, remain poorly understood.

Synthesized silicon NWs (SiNWs) represent an extensively studied doped NW structure (6, 7, 9), can be compared directly to lithographically defined nanoscale silicon devices that are the standard of the semiconductor industry (10). Previous investigations have shown that basic *p*- and *n*-channel field-effect transistors (7, 9) as well as more complex axial and radial modulation doped structures including *p*/*n* diodes (11, 12) could be realized. However, measurements in smaller diameter *p*-Si NWs have yielded room-temperature hole-mobilities (7) and low-temperature transport behavior (13, 14) consistent with clean, intrinsic material and not that expected for a nanostructure with the same effective dopant concentration homogeneously distributed within the NWs.

These latter results suggest that dopants may be inhomogeneously distributed in the radial direction, and moreover, that the distribution may depend on NW diameter. Theoretical studies suggest a tendency toward surface doping in molecular diameter *p*- and *n*-Si NWs (15, 16) that are considerably smaller than structures used to fabricate most reported NW devices. Direct experimental determination of dopant location in NWs is challenging, although there has been recent progress (17–21). For example, high-resolution secondary ion mass spectroscopy was used to probe for gold-impurities in μm diameter Si wires with a depth resolution of $\approx$20 nm (17), and atom probe tomography has been used to investigate the distribution of impurity atoms in Si NWs with nanometer resolution (18, 19). The vertical geometry needed for these latter measurements may, however, place limitations on growth conditions that yield NWs suitable for analysis. In addition, Raman scattering studies of 80–100-nm diameter Si NWs have indicated that active boron dopants are located only at the surface with higher concentrations remote to the active growth tip, suggesting that dopant incorporation occurs by homogeneous surface deposition during axial NW elongation (20, 21). Here, we characterize the distribution of electrically active *n*- and *p*-type dopants as function of diameter in Si and Ge NWs synthesized by the nanocluster catalyzed VLS approach (6–9). Our method (Fig. 1) is based on one or more cycles of controlled nanometer-scale low-temperature NW surface oxidation and selective surface oxide etching, followed by electrical transport measurements made with NWs configured as field-effect transistors (FETs). Low (<100 °C) temperature oxidation and etching precludes thermal diffusion or segregation of dopants after NW synthesis (1, 21). This approach can distinguish uniform dopant incorporation versus surface segregation of dopant because an oxidation/etch cycle will yield a relatively small change in FET properties for uniformly doped NW, whereas removal of surface dopant, which leaves a nominally intrinsic (undoped) NW, will manifest a large change in device threshold voltage.

The growth conditions for doped Si and Ge NWs were optimized to achieve axial nanocluster-catalyzed growth without measurable competing homogeneous decomposition and surface overcoating as described in ref. 11. Experimentally, these conditions were confirmed from scanning electron and transmission electron microscopy images, which exhibit uniform diameter and crystalline structure extending to the outer surface (11). In contrast, tapered nanowire structures (20, 21), which are formed by surface overcoating during axial elongation, were not investigated because dopant incorporation by homogenous surface deposition is a distinct process and could lead to an

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[1]To whom correspondence should be addressed. E-mail: cml@cmliris.harvard.edu.

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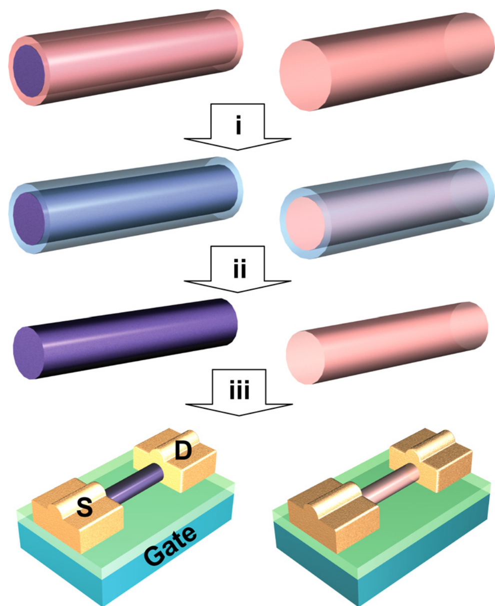

Fig. 1. Overview of experimental method. Shown are the sequence of steps used to investigate dopant location in surface (bulk) doped nanowires, including (i) controlled oxidation of the nanowire surface, (ii) etching to remove the surface oxide, and (iii) device fabrication. Pink shaded areas indicate regions where dopant is located.

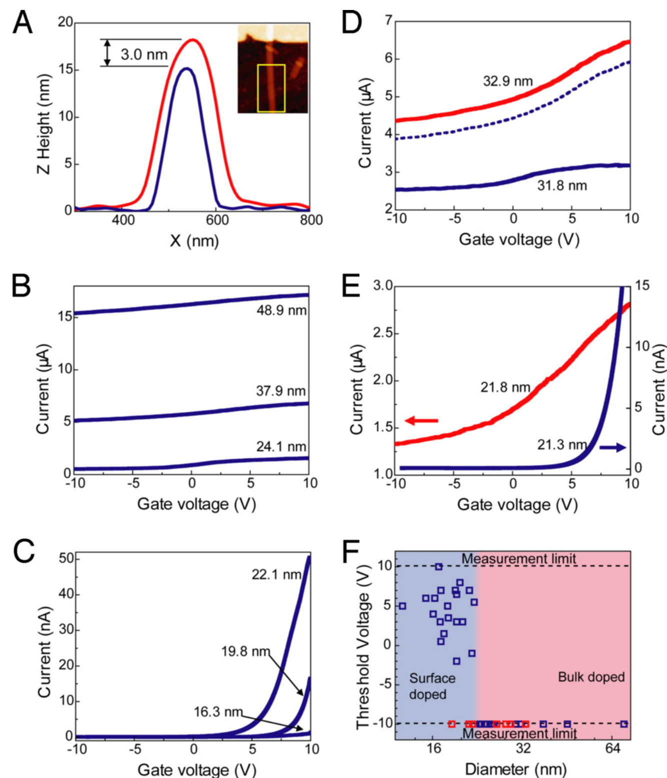

Fig. 2. Diameter-dependent transport behavior of *n*-type Si NWs. (*A*) Averaged cross-sectional height profiles determined from AFM images before (red) and after (blue) oxidation and etching of a NW. (*Inset*) the topographical AFM image, the yellow rectangle indicates the ≈500 nm × 1,000 nm averaging area. (*B* and *C*) Series of I–V_g curves at V_{sd} = 1 V measured from NWs after oxidation and etching with different as-grown diameters. I–V_g curves at V_{sd} = 1V measured from large (*D*) and small (*E*) diameter control NWs (red) and NWs after (solid blue) oxidation and etching. The blue dashed line in *D* is the I–V_g curve calculated from the control NW (red line) after a single oxidation/etching cycle based on a uniform bulk doping model. The diameters labeled in *B*–*E* for blue curves are as-grown diameters before the oxidation and etching process; the diameters for red curves correspond to diameter of the control NW. (*F*) Diameter dependence of threshold voltage. Blue (red) squares represent data from NWs after oxidation and etching (control NWs). The blue (pink) shaded areas highlight diameters of NWs that do (do not) exhibit clear depletion behavior after a single oxidation/etch cycle.

unintentional enhancement of dopant concentration at the NW surface. We do note that controlled homogenous deposition of radial shells (22) is an effective synthetic approach for creating doped NW structures, including those with electrically active junctions (12).

Results and Discussion

Atomic force microscopy (AFM) data recorded from a phosphorus-doped (*n*-type) Si NW before and after 1 cycle of chemical oxidation and etching (Fig. 2*A*) show a 3.0-nm reduction in height. The large apparent change in width (Fig. 2*A*) is due to tip-induced broadening (23) and changes in the AFM tip before and after the oxidation/etching process. Analysis of cross-sectional data recorded from a sampling of 7 *n*-type SiNWs yields average ± 1SD reduction in diameter of 4.1 ± 0.9 nm of SiO_2, which corresponds to removal of ≈3–4 atomic layers (≈0.9 nm) of Si during the native oxide etch and single oxidation/etch cycle. For clarity, the term diameter in this paper always refers to the initial as-grown diameter unless otherwise specified.

We have characterized the electrical properties of 15–70-nm diameter *n*-type Si NWs after the single oxidation/etch cycle in a field effect transistor (FET) configuration in vacuum. These data (Fig. 2 *B* and *C*) exhibit 2 distinct classes of behavior depending on NW diameter. Current (I) versus gate-voltage (V_g) for devices with larger, > ≈25-nm diameter NWs all exhibit relatively high conductances, and none of these FETs can be depleted within the ± 10 V accessible V_g window. In contrast, devices with smaller, < ≈22-nm diameter NWs (Fig. 2 *C* and *E*) exhibit dramatic change after a single oxidation/etch cycle: the NW FETs show well-defined threshold voltage (V_{th}) with V_{th} > 0 on average and an on-current typically 10–100 times lower than larger diameter NWs.

Comparison of *n*-Si devices fabricated from control NWs and those following a single oxidation/etch cycle further highlights these diameter-dependent differences. Specifically, I–V_g data from devices fabricated with an ≈32-nm diameter control NW and one following a single oxidation/etch cycle (Fig. 2*D*) are similar except for the ≈2× reduction in conductance. The I–V_g curve calculated from the control NW data assuming a uniform dopant distribution and decrease in channel cross-section because of oxidation/etch does, however, yield a larger conductance than observed experimentally. This calculation indicates that the surface dopant concentration is enriched in the larger diameter *n*-Si NWs, although the NW FETs still behave as a heavily doped depletion mode devices after removal of this surface layer. The similar dopant surface segregation in an ≈60-nm diameter NWs has been reported recently on the basis of scanning photocurrent microscopy, transport measurement and atom probe tomography (19). In contrast, I–V_g data recorded from devices with an ≈22-nm diameter single oxidation/etch and control NWs (Fig. 2*E*) highlight a well-defined positive V_{th} and much lower on-current after a single oxidation/etch cycle.

A summary of data recorded from 42 distinct *n*-type Si NW FET devices (Fig. 2*F*) illustrates clearly these 2 distinct classes and shows that the behavior for NWs with diameters > or < ≈23 nm is robust. Specifically, these data show that V_{th} changes sharply from beyond the measurement limit (−10 V) to a positive value ≈23-nm diameter. In addition, control NW devices with diameters as small as 18 nm (red squares, Fig. 2*F*), which have not undergone an oxidation/etch cycle, exhibit

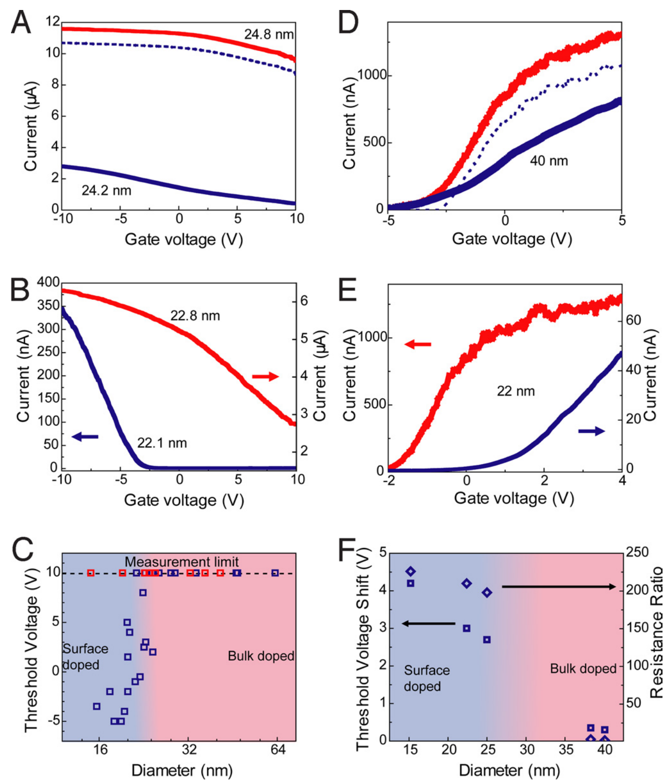

Fig. 3. Diameter-dependent transport behavior of *p*-type Si and *n*-type Ge NWs. (*A* and *B*) I–V_g curves at V_{sd} = 1 V measured from as grown *p*-Si NWs (red) and NWs after a single oxidation/etch cycle (solid blue). (*C*) Diameter dependence of threshold voltage for *p*-Si NWs. Blue and red squares represent data from *p*-Si NWs after oxidation/etch cycle and as-grown NWs, respectively. The blue (pink) shaded areas highlight diameters of NWs that do (do not) exhibit clear depletion behavior after a single oxidation/etch cycle. (*D* and *E*) I–V_g curves at V_{sd} = 1 V for same *n*-GeNWs before (red) and after (solid blue) etching. Blue dashed lines in *A* and *D* are I–V_g curves calculated from the control (red lines) based on the uniform bulk doping model. (*F*) Diameter dependence of V_{th} and resistance ratio for *n*-Ge NWs. The blue (pink) shaded areas highlight diameters of *n*-Ge NWs that do (do not) exhibit large threshold voltage shift and resistance ratio after removal of a thin surface layer. All diameters labeled in this figure are as-grown diameters.

characteristics similar to heavily doped *n*-type devices and the larger diameter NWs. This shows that the substantial change in transport properties can be associated with removal of the surface layer in the small diameter NWs. We attribute these results primarily to diameter-dependent dopant incorporation during growth, and discuss this versus other mechanisms below after presenting additional data demonstrating the generality of this phenomenon for other NW systems.

We have also characterized the diameter-dependent behavior of *p*-type Si and *n*-type Ge NWs. Results from as-grown and oxidized/etched (≈0.5-nm thick Si layer removed) boron doped *p*-type Si NWs show comparable behavior as a function of diameter as *n*-Si NWs. For example, I–V_g data from an ≈25-nm diameter as-grown and etched NWs (Fig. 3*A*) are similar except for the ≈4× reduction in conductance for the etched NW. The calculated I–V_g curve for the etched NW based on the as-grown data shows a larger conductance than observed experimentally, which is consistent with higher concentration of dopant at the surface. The transport behavior of larger diameter etched *p*-Si NW FETs is, however, consistent with heavily doped depletion mode devices (i.e., no V_{th} within a V_g window of ±10 V) after removal of the surface layer. Representative I–V_g data recorded from devices with an ≈22-nm diameter (Fig. 2*B*) exhibit distinctly different characteristics after the oxidation/etch cycle with a well-defined V_{th} and one order of magnitude lower on-current. The reproducibility of these results and clear transition between large and small diameter NWs can be seen in the plot of data from 33 *p*-Si NW devices (Fig. 3*C*), where a well-defined V_{th} is observed in devices with diameters <23 nm after etching. As-grown, control NW devices with diameters as small as 15 nm exhibit characteristics similar to heavily doped *n*-type devices and the larger diameter *p*-Si NWs, and thus demonstrate that the transition can be associated with removal of the surface layer in the small diameter *p*-Si NWs.

The generality of these results was further assessed through studies of *n*-type Ge NWs. Ge represents an attractive experimental system because water soluble GeO_2 can be readily removed in situ without degrading the device contacts, thus allowing for direct comparison of the same NW device before and after oxidation/etching. We were careful to optimize Ge NW synthesis for the diameters investigated to realize axial growth without radial overcoating to avoid complications from the latter in the analysis of dopant incorporation. A typical large, 40-nm diameter NW (Fig. 3*D*) exhibited a 2× decrease in channel conductance with little change in V_{th} after etching. The drop in conductance is, however, greater than expected for a reduction in cross-section and indicates that dopant concentration is higher at the surface of the Ge NWs. In contrast, a representative small, 22-nm diameter NW (Fig. 3*E*) showed a >20-fold drop in conductance and an ≈3 V shift in V_{th} after etching. A summary of data from 5 devices (Fig. 3*F*) shows a transition in V_{th} at ≈25–30 nm, although the relatively small number of devices makes this cross-over diameter less certain than for *n*- and *p*-Si NWs. In addition, we have compared the resistance ratio (after/before etching) at V_g = 0 because the measurements were made on the same devices. These data (Fig. 3*F*) also show clearly the distinct behaviors between large vs. small diameter Ge NWs.

Our investigations of *n*-Si, *p*-Si, and *n*-Ge NWs show that there is a distinct diameter-dependent transition in electrical transport behavior after removal of the surface region of NWs by low-temperature oxidation and etching. In small diameter NWs, removal of the surface layer yields device characteristics with carriers depleted at V_g = 0 V, whereas large diameter NWs exhibit properties of heavily doped material. Over the entire range of diameters studied, 15–70 nm, all NWs showed characteristics of heavily doped semiconductor before oxidation and etching. Hence, the substantial change in transport properties can be associated with removal of the surface layer in the small diameter NWs. These diameter dependent results could arise from several factors, including (i) diameter-dependent dopant incorporation during growth, (ii) dielectric confinement (24, 25), and (iii) surface depletion (26, 27), although results indicate that (i) is the dominant factor. The dielectric confinement model predicts that dopant ionization energy will increase with decreasing NW diameter, which could deplete small diameter NWs. Studies of surface depletion, which arises from carrier trapping at the Si/SiO_x (or Ge/GeO_x) interface, also suggest a diameter dependent change in V_{th} as the diameter of NWs is reduced. However, the effects due to both dielectric confinement and surface depletion are determined only by the final diameter of the NW FETs, unless there is diameter dependent dopant incorporation. Hence, the sharp transition we observed together with the absence of a transition in control NWs over the entire range of diameters strongly indicates the existence of diameter dependent dopant incorporation. It worth noting that NWs over the diameter range (15–70 nm) investigated in our work have a mixture of <110>, <111>, and <112> growth axes (28), and thus it is unlikely that the observed transition is due to the diameter dependent surface reconstruction, which could depend on the crystallographic orientation at the surface (16).

To address further the diameter-dependent dopant distribution and these models we have also carried out measurements on *n*-Si

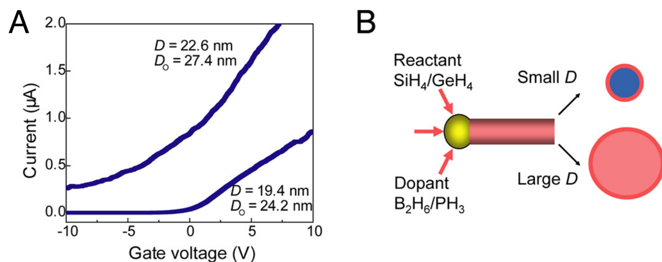

Fig. 4. Diameter dependent dopant distribution. (*A*) Comparison of I–V_g curves at V_{sd} = 1 V between different diameter n-type Si NWs after 4 cycles of oxidation and etching. *D* (D_0) is the diameter after (before) oxidation and etching. (*B*) Schematic of dopant distribution. Pink and dark pink shaded parts together represent heavily doped regions, with darkness of the pink color indicating the relative dopant concentration (darker = higher), and blue corresponds to intrinsic region.

NWs after multiple oxidation/etch cycles. Representative I–V_g curves recorded from NWs with as-grown diameters slightly larger than and approximately the same as the transition point after 4 cycles of oxidation and etching (Fig. 4*A*) show several important features. The NW with as-grown diameter at the transition point of 24 nm exhibits, as expected, switch to enhancement mode after the 4 oxidation/etching cycles, where the final diameter is 19.4 nm. The NW device with as-grown diameter of 27.4 nm, which is several nm larger than the observed transition diameter, and final diameter after 4 oxidation/etch cycles of 22.6 nm, which is less than or equal to transition diameter, could not be turned off and exhibited a relatively large current over the entire V_g window. This behavior is consistent with a heavily doped FET even after etching to below the transition diameter. Importantly, these data confirm that the major contribution to the diameter-dependent transition is not associated with surface depletion or dielectric confinement, which would manifest itself independent of initial starting diameter, but rather is due to diameter-dependent dopant incorporation.

These multicycle oxidation/etch data together with the results presented earlier for Si and Ge NWs are summarized schematically in Fig. 4*B*. During nanocluster-catalyzed VLS growth of small diameter Si and Ge NWs, the active dopants segregate in the ≈1–2-nm surface region whereas the remaining bulk of the NW is effectively free of active dopants. During the corresponding growth of larger diameter NWs, there is an enrichment of dopants in the surface region but the bulk of the NW also contains dopants. Several models for dopant surface segregation in nanostructures have been proposed (5, 15, 16, 29). First, "self-purification" driven dopant surface segregation has been reported in nanoparticles during nucleation (5) or annealing (29). This model cannot explain the present results because (i) nucleation occurs only at the initial stage of NW elongation and (ii) NW growth temperatures are far below those where dopant diffusion would be significant (1). Second, the energy for a dopant may be lower at the surface versus bulk because of lattice relaxation, although calculations suggest that this energy difference should only become important in the molecular size limit (15, 16). Third, surface reconstruction could also lower the energy of dopant at the surface versus bulk, and notably, calculations suggest that the energy scale (>100 meV) is compatible with segregation at growth temperatures (16). Qualitatively, this mechanism could yield a diameter dependent transition in dopant incorporation: When the NW diameter is small all dopants can be accommodated at the reconstructed surface with an intrinsic core, but as the surface to volume ratio decreases all dopants cannot be accommodated at the surface and there is a transition to bulk doped material. However, further experimental and theoretical studies will be needed to confirm any detailed mechanism and to provide quantitative explanation of the transition diameter.

Conclusions

We have defined the diameter-dependent location of electrically active dopants in Si and Ge nanowires prepared by nanocluster-catalyzed VLS growth without measurable surface overcoating. The location of active dopants assessed from electrical transport measurements before and after removal of controlled thicknesses of material from NW surfaces by low-temperature chemical oxidation and etching show a well-defined transition from bulk-like to surface doping as the diameter is decreased <22–25 nm for *n*- and *p*-type Si NWs. Similar diameter-dependent results were also observed for *n*-type Ge NWs, suggesting that surface dopant segregation may be general for small diameter NWs synthesized by the VLS approach. There are also important implications of the observed diameter-dependent dopant incorporation independent of the specific mechanism. First, our results can explain the enhanced electrical performance of small diameter Si NWs in which low-temperature studies showed clean structures on length scales up to at least 400 nm and more than an order of magnitude longer than top-down fabricated NW structures (13, 14). The uniform transport properties in chemically synthesized small-diameter NWs can now be attributed to the preferential segregation of dopant at the surface, which minimizes potential fluctuations because of ionized dopant impurities. Second, the surface segregation of dopant in small diameter NWs is an ideal realization of delta doping (30), which is proposed to overcome the critical problem of random dopant fluctuations in aggressively scaled top-down fabricated metal-oxide-silicon field effect transistors (MOSFETs). The natural spatial separation of dopants in a cylindrical surface layer of small-diameter NWs is an ideal doping geometry and could open up opportunities for exploring high-mobility, scaled NW FETs as well as low-temperature studies of one-dimensional electron and hole gases.

Materials and Methods

Nanowire Synthesis. NWs were synthesized by gold nanocluster catalyzed chemical vapor deposition as described (7, 9). The *n*-type Silicon NWs (SiNWs) are synthesized at 435 °C at 30 Torr pressure with 3 standard cubic centimeters per minute (sccm) silane as Si source, phosphine (0.1% in H_2) as *n*-type dopant source and 60 sccm H_2 as carrier gas. The flow rate of phosphine varies from 3 sccm to 10 sccm to achieve feed-in ratio from 1,000:1 to 300:1 (Si:P) and the growth time is 60 min. *p*-type SiNWs are synthesized at 440 °C at 30 Torr with 2.5 sccm silane, 4.1 sccm to 12.5 sccm 100 ppm diborane in He (Si:B = 3,000:1–1,000:1) and 10 sccm Ar, and the growth time is 30 min. *n*-type germanium NWs (GeNWs) are synthesized at 280 °C at 400 Torr with 10 sccm 10% GeH_4, 10 sccm 0.1% PH_3, and 200 sccm H_2 (Si:*P* = 100:1), the growth time is 30 min. Growth conditions were optimized to minimize the overcoating because of the noncatalytical decomposition of precursors. Transmission electron microscopy (TEM) images demonstrated that the synthesized NWs used in these studies had uniform diameters, thus verifying the absence of homogeneous radial deposition during axial nanowire elongation as described in ref. 11.

NW Surface Oxidation and Etching. The *n*-type Si NW growth wafer was first etched with 1% HF for 1 min. to remove the native oxide layer. Subsequent cycles of chemical oxidation/etching were carried out: oxidation in boiling 1:1:6 $HCl:H_2O_2:H_2O$ solution 20 min (31), and then etching with 1% HF for 1 min. When multiple cycles of oxidation/etching were used to reduce the diameter, each subsequent cycle was carried out immediately after the 1% HF etch step to avoid formation of new native oxide. Control samples for *n*-type Si NWs were prepared by 1% HF etching (1 min) immediately after growth. The first cycle for *p*-type SiNWs consisted of native oxide growth for 24 h in a cleanroom followed by 1% HF etching for 1 min. The control sample for the *p*-type Si consisted of as-grown NWs with native oxide because the threshold voltage transition can be clearly observed after native oxide etching. Because both oxidation and etching reactions for Si are self-limiting (31, 32), the thickness of the removed surface layer is uniform. This etching condition is known to produce Si NWs with surface smoothness comparable if not better than as-grown Si NWs (33). The *n*-type Ge NWs were oxidized and etched in a continuous process using 0.02% H_2O_2 solution; a single step involved etching for 5 s followed by rinse with deionized H_2O.

NW Diameter Characterization. NW diameters were measured by atomic force microscopy (AFM). All AFM data are taken by a Digital Instruments Nanoscope IIIa Multimode AFM at tapping mode using PPP-NCH AFM tip from NanoSensors. Typically, 3.5 μm $\times$ 3.5 μm images were recorded with an x-scan frequency of 2 Hz at 512 $\times$ 512 pixel density using tip-tune amplitude of 1–1.5 V, amplitude setpoint of 0.8–1.2 V, feedback integral gain of 0.8–1.5, and feedback proportional gain of 1–3. To measure the diameter change after oxide removal for the same Si NW, the NW was fixed at 1 end by a Cr/Au pad defined by electron beam lithography (EBL) on a ZrO_2/Si substrate. Because Cr/Au and ZrO_2 are stable in both 1:1:6 HCl:H_2O_2:H_2O and 1% HF solution, the same NW can be located after etching and there will be no artifacts contributing to diameter change from etched substrate. AFM images were recorded before and immediately after the 1% HF etch step. The NW diameter was determined from the height change in the cross-sectional profile averaged $>$ $\approx$1 μm along the NW axis, where a local plane was fit to the substrate in this region. AFM data for Ge NWs were obtained directly from working devices before and immediately after etching because the source/drain contacts were stable to the Ge etching solution.

The measured diameter changes associated with native oxide removal in *n*-type and *p*-type Si NWs were 1.8 $\pm$ 0.8 and 2.2 $\pm$ 1.2 nm, respectively, corresponding to the removed surface Si thickness of 0.4 and 0.5 nm respectively (radius change, converted by factor 0.44, SiO_2 to Si) (34). The diameter change due to removal of chemical oxide on *n*-type Si NWs was 2.3 $\pm$ 0.4 nm (0.5 nm Si thickness) and H_2O_2 etching of Ge NWs was 2.5 $\pm$ 1.3 nm. The values were based on averages $>$7, 7, and 6 independent NWs for the cases of *n*-Si, *p*-Si, and *n*-Ge, respectively. The native and chemical oxide thicknesses determined from our measurements on SiNWs were comparable to those values obtained from studies of planar Si wafers (31, 34).

Device Fabrication and Measurements. NW suspensions in isopropanol were deposited on 60-nm ZrO_2 coated degenerately doped silicon wafer (☜ orientation, 0.005 Ω-cm, Silicon Valley Microelectronics). Contact electrodes are defined by e-beam lithography and metal evaporation (Ni for SiNWs and Ti for GeNWs), where the native oxide on NW under contact is etched by BHF for 5 s immediately before being loaded into the metal deposition system. Devices are annealed in forming gas (380 °C 2 min. for Ni-Si and 330 °C 30 s for Ti-Ge) before measurement to reduce both contact resistance (35) and interfacial trap states (34). All electrical measurement is performed in Desert probe station (Desert Cryogenics) at room temperature, 10^{-5} torr base pressure. I–V_g curve was recorded at 1 V source drain voltage; $\pm$10 V measurement limit of gate voltage is set by the maximum voltage ZrO_2 film can hold ($<$1 nA leakage). The hysteresis induced V_{th} uncertainty in I–V_g curve is reduced to negligible level by annealing and vacuum as illustrated in Fig. S1.

Surface Depletion. Surface depletion is a general phenomenon expected in planar (34) and NW (26, 27) devices because of states at the Si/SiO_x interface that trap carriers. The thickness of the surface depletion layer is governed by the interface trap density and dopant/carrier concentration (26, 34). In our experiments, the dopant concentration estimated from I–V_g data are from 0.5–1.7 $\times$ 10^{20}/cm^3 for large diameter Si NWs after 1 oxidation/etching cycle, and yields—even for a very high interface trap density 2 $\times$ 10^{12}/eV/cm^2 (27)—a depletion thickness $<$1 nm (26). The lack of a threshold voltage transition in the control NWs (without etching) down to a diameter of 15–18 nm is consistent with this analysis. A larger depletion could occur after the first oxidation/etching cycle if the dopant concentration is much lower, although this would simply yield a monotonic shift of threshold voltage with decreasing diameter in contrast to the sharp transition we observe. We thus conclude that surface depletion alone cannot yield the observed sharp transition at a diameter of $\approx$23 nm.

Diameter-Dependent Device Response. Assuming a uniform dopant distribution and unchanged mobility after oxidation/etching for large diameter NWs, the I–V_g curve after oxidation and etching can be estimated from the control group NW I–V_g data through the geometrical reduction of the cross-sectional area and gate capacitance as:

$$I(V_g) = I_0(0)\left(\frac{D}{D_0}\right)^2 + [I_0(V_g) - I_0(0)]\,\frac{C_{gate}}{C_{0,gate}}$$

where $C_{gate} = 2\pi\varepsilon\varepsilon_o L/\cosh^{-1}(2h/D)$ (36), and D, C_{gate}, and L are the diameter, gate capacitance and channel length of NW respectively and h is the thickness of gate dielectric. Because the doping concentration for our large diameter NW is relatively high, the effects of contact resistance, surface depletion and electron affinity differences can be ignored. This equation is also applicable to estimating I–V_g curves after several oxidation/etch cycles as long as these assumptions are valid.

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