LETTER

doi:10.1038/nature09749

Programmable nanowire circuits for nanoprocessors

Hao Yan[1]*, Hwan Sung Choe[2]*, SungWoo Nam[3]*, Yongjie Hu[1], Shamik Das[4], James F. Klemic[4], James C. Ellenbogen[4] & Charles M. Lieber[1,3]

A nanoprocessor constructed from intrinsically nanometre-scale building blocks is an essential component for controlling memory, nanosensors and other functions proposed for nanosystems assembled from the bottom up[1–3]. Important steps towards this goal over the past fifteen years include the realization of simple logic gates with individually assembled semiconductor nanowires and carbon nanotubes[1,4–8], but with only 16 devices or fewer and a single function for each circuit. Recently, logic circuits also have been demonstrated that use two or three elements of a one-dimensional memristor array[9], although such passive devices without gain are difficult to cascade. These circuits fall short of the requirements for a scalable, multifunctional nanoprocessor[10,11] owing to challenges in materials, assembly and architecture on the nanoscale. Here we describe the design, fabrication and use of programmable and scalable logic tiles for nanoprocessors that surmount these hurdles. The tiles were built from programmable, non-volatile nanowire transistor arrays. Ge/Si core/shell nanowires[12] coupled to designed dielectric shells yielded single-nanowire, non-volatile field-effect transistors (FETs) with uniform, programmable threshold voltages and the capability to drive cascaded elements. We developed an architecture to integrate the programmable nanowire FETs and define a logic tile consisting of two interconnected arrays with 496 functional configurable FET nodes in an area of ~960 μm^2. The logic tile was programmed and operated first as a full adder with a maximal voltage gain of ten and input–output voltage matching. Then we showed that the same logic tile can be reprogrammed and used to demonstrate full-subtractor, multiplexer, demultiplexer and clocked D-latch functions. These results represent a significant advance in the complexity and functionality of nanoelectronic circuits built from the bottom up with a tiled architecture that could be cascaded to realize fully integrated nanoprocessors with computing, memory and addressing capabilities.

The programmable nanowire FETs (NWFETs) incorporated a top-gated geometry (Fig. 1a, left panel) using Ge/Si core/shell nanowires as the semiconductor channel because previous work[12] had shown that this provided high yields of devices with uniform threshold voltages and on-current characteristics. To realize programmable, non-volatile NWFETs, we implemented a trilayer Al_2O_3–ZrO_2–Al_2O_3 dielectric structure (Fig. 1a, right-hand panels) for charge trapping[13]. For a p-type Ge/Si nanowire channel, negative trapped charges increase the hole density (Fig. 1a, top right) and positive trapped charges decrease the hole density (Fig. 1a, bottom right) in the channel. The modulation of carrier density by trapped charges shifts the threshold of the NWFET in a predictable and non-volatile manner. We grew the Al_2O_3–ZrO_2–Al_2O_3 dielectric structure by atomic-layer deposition after fabrication of metallic source and drain nanowire contacts (Methods). A cross-sectional transmission electron microscopy image recorded from a representative device (Fig. 1b) shows that our NWFET device consists of the designed structure with a 10-nm-diameter germanium nanowire core, a 2-nm-thick concentric silicon shell and conformal 2-nm Al_2O_3, 5-nm ZrO_2 and 5-nm Al_2O_3 layers.

The gate response of a NWFET with a trilayer dielectric was characterized in a device with six gate lines, a 1 × 6 node element (Fig. 1c, inset). For these measurements, we used one gate line as the active gate and the other gate lines were grounded. The drain–source current, I_{ds}, recorded as a function of drain–source voltage, V_{ds}, for different values of gate voltage, V_{gs} (Fig. 1c), has the behaviour expected of a p-type depletion-mode FET[14]. The conductance–V_{gs} curves of the same device with ±6-V (Fig. 1d, blue) and ±9-V (Fig. 1d, red) sweeps in V_{gs} show anticlockwise hysteresis loops that agree well with the charge-trapping mechanism[15]. The hysteresis window increases by ~2 V in the ±6 to ±9-V V_{gs} sweeps, which is consistent with more charge being trapped at larger voltages and the charge-trapping model[13]. Significantly, these data demonstrate that two distinct states are observed. After a gate bias of −6 V, the conductance of the NWFET changed by >10^3 as V_{gs} varied between 0 and 2 V; in contrast, after a

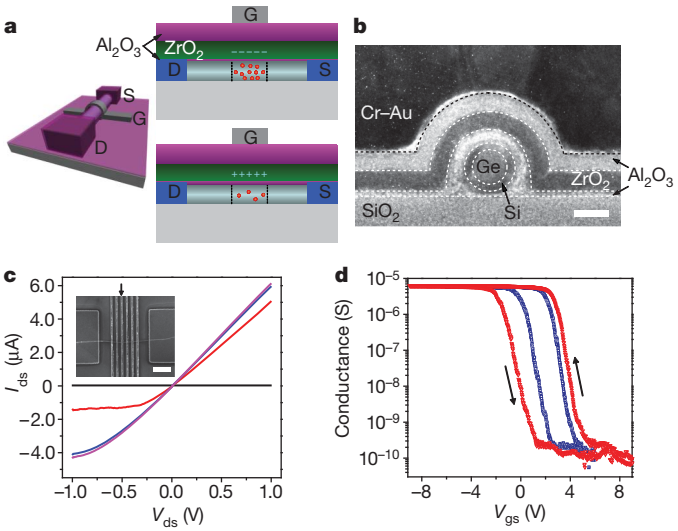


Figure 1 | Structure and characterization of the programmable NWFET. **a**, Left: schematic of the top-gated NWFET; S, D and G correspond to source, drain and gate, respectively. Right: representative hole concentration in a p-type Ge/Si NWFET for two charge-trapping states illustrating carrier accumulation for a negative trapped charge (top right) and depletion for a positive trapped charge (bottom right) in the ZrO_2 layer. **b**, Cross-sectional transmission electron microscopy image of a representative nanowire device, with substrate surface (SiO_2) and gate (Cr–Au) at the bottom and the top of the image, respectively. Other components of the nanowire and dielectric layers are labelled, and dashed lines define the boundary between different components. Scale bar, 10 nm. **c**, I_{ds}–V_{ds} curves recorded from a six-gate NWFET with V_{gs} = 8 (black), 3 (red), 0 (blue) and −8 V (magenta) (G3), and G1, G2, and G4–G6 grounded. Inset, scanning electron microscopy image of the device. The small black arrow indicates G3. Scale bar, 1 μm. **d**, Semi-logarithmic plot of conductance versus V_{gs} for the same device as in **c**, recorded for ±6-V (blue) and ±9-V (red) sweeps at V_{ds} = 0.5 V; arrows represent sweep/hysteresis direction.

[1]Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts 02138, USA. [2]Department of Physics, Harvard University, Cambridge, Massachusetts 02138, USA. [3]School of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts 02138, USA. [4]Nanosystems Group, The MITRE Corporation, McLean, Virginia 22102, USA.
*These authors contributed equally to this work.

gate bias of +6 V, the conductance change was less than 50% over the same V_{gs} range. We thus define the former state as 'active', because the NWFET behaves like an active transistor, and define the latter state as 'inactive', because the device behaves like a passive interconnection. Neither programmed state shows degradation on the timescale of a day (Supplementary Fig. 1). The stable programmability of individual NWFETs between the active and inactive states allows distinct functional circuits to be realized from arrays as described below.

We initially investigated the potential of these multi-input programmable NWFETs for building integrated circuits with two coupled nanowire elements (Fig. 2a, left panel), where the first element, NW1, had four independently configurable input gates, G1–G4, and the second element, NW2, had a single input gate connected to the output (drain) of NW1. In this demonstration, the first and third gate nodes of NW1 and the gate node of NW2 were set to the active state (Fig. 2a, green dots), and the other gate nodes were set to the inactive state (Methods). With source voltages of 2.5 and 3 V applied to NW1 and NW2, respectively, input G1 was switched between 0 and 1 V while G2–G4 were held at 0 V (Fig. 2a, top right). Notably, simultaneous measurements of the output voltage from NW1, V_{IG}, and NW2, V_{out}, with the 0- and 1-V G1 input variations (Fig. 2a, lower right), show that V_{IG} is switched between high (2.2-V) and low (0.2-V) levels and that V_{out} is toggled between low (0.6-V) and high (3.0-V) levels. Similar switching of the V_{IG} and V_{out} levels was recorded when the input to the other active node, G3, was varied and G1, G2, G4 held at 0 V. However, no switching of the V_{IG} and V_{out} levels was observed when the input voltage on either of the inactive input nodes, G2 and G4, was changed from 0 to 1 V. These results show that our programmable NWFET functions as a transistor switch in its active state and that multiple switches can be coupled together by feeding the output of one FET into the input gate of another, and thus suggest that assembly of programmable NWFETs into a suitable architecture could yield integrated circuits capable of processing.

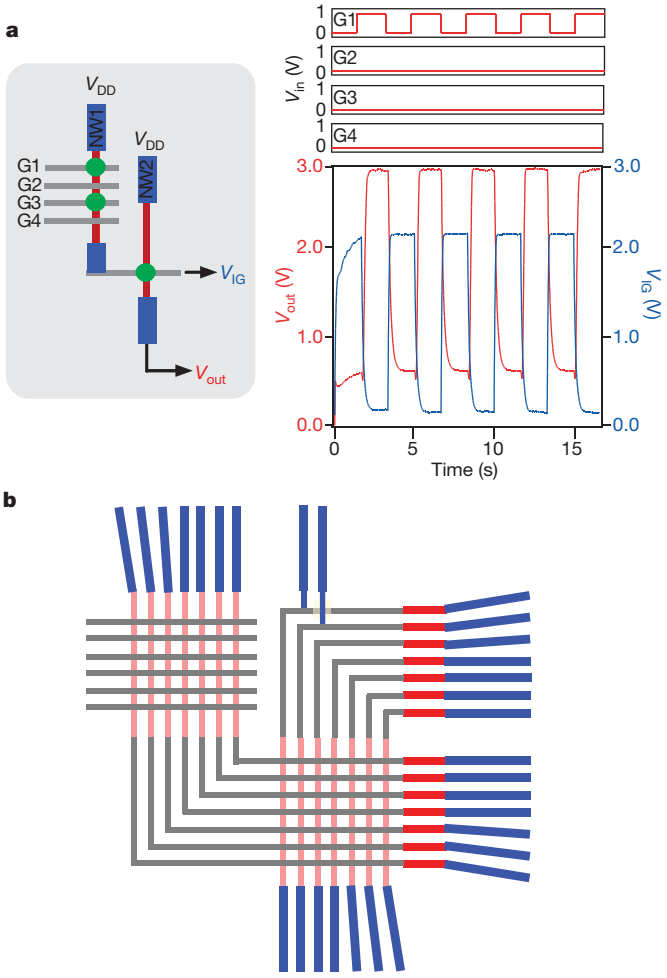
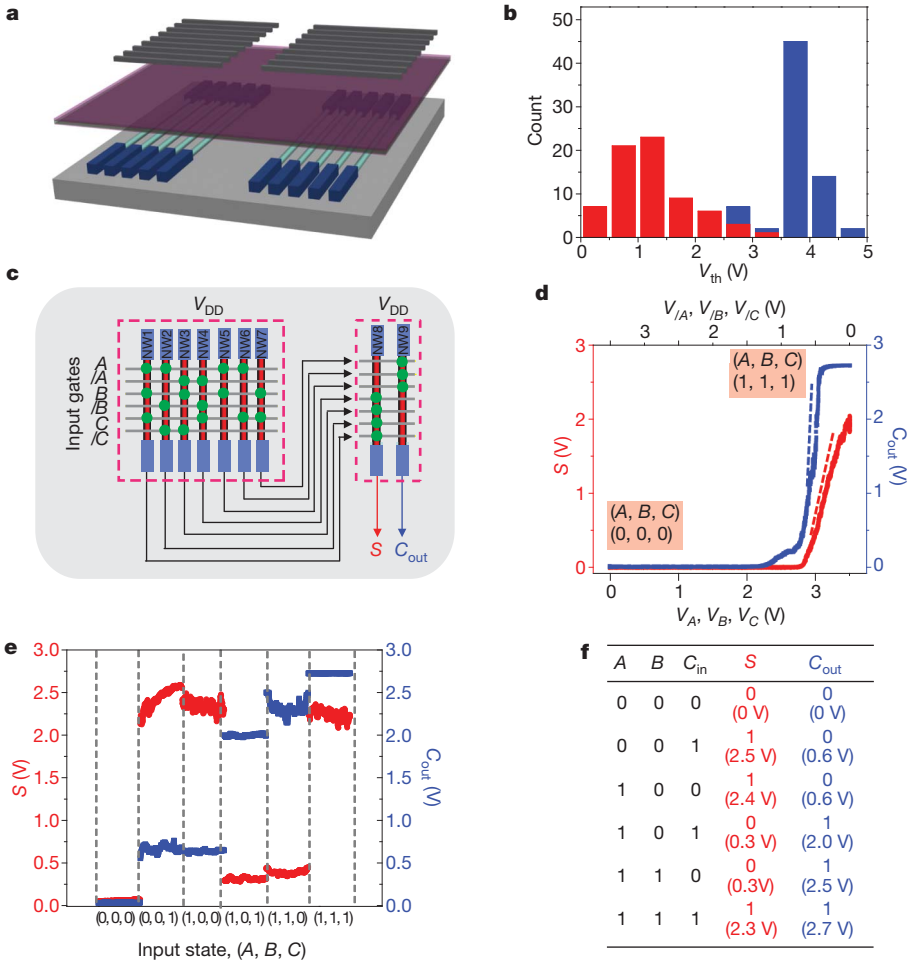


Figure 2 | Coupled NWFET devices and PNNTA architecture. **a**, Characterization of a nanowire–nanowire, coupled multigate device. Left: schematic of the device. Green dots indicate the gate nodes that were programmed as an active state. Top right: input signals to G1–G4. Bottom right: output signals from NW1 (V_{IG}, blue) and NW2 (V_{out}, red). **b**, Design of the unit logic tile for integrated nanoprocessors containing two PNNTAs, block 1 (upper left) and block 2 (lower right), comprising charge-trapping nanowires (pink) and metal gate electrodes (grey). The PNNTAs are connected to two sets of load devices (red). Lithographic-scale electrodes (blue) are integrated for input and output. Each PNNTA provides programmable logic functionality of up to approximately eight distinct logic gates. More-complex logic functions can be computed through the hierarchical interconnection of unit logic tiles in linear arrays (Supplementary Fig. 2).

To exploit the unique properties of our programmable NWFETs, while simultaneously recognizing assembly limitations, we have developed a scalable system architecture in which both the locations and the interconnections of transistors are decided after fabrication. This architecture was formulated with the concept of building extended nanoprocessor systems consisting of arrays of interconnected logic tiles[10,16] (Supplementary Fig. 2). The unit logic tile (Fig. 2b), refined both by extensive simulation[11] and by experiment, consists of two programmable, non-volatile nanowire transistor arrays (PNNTAs). The tile is sized to be able to execute a program equivalent to a small number of logic gates, and functions as follows. Metal electrodes are used to gate nanowires in the block-1 PNNTA (Fig. 2b, upper left), and the output of the nanowires is connected by metal electrodes to static load devices. By programming selected nanowire gate nodes to the active transistor state, NOR logic gates[5] can be mapped into block 1. The outputs of this NOR logic circuit are passed over and used as gate inputs to the block-2 PNNTA (Fig. 2b, lower right) that is also programmed with NOR logic gates. In this way, the outputs of the logic circuits in block 1 can be used to drive the circuit in block 2, thus making it possible to form two-level networks of logic gates in the unit tile that represent arbitrary Boolean functions.

We realized the key architectural tile by fabricating PNNTAs as shown schematically in Fig. 3a (Methods). Briefly, a parallel array of Ge/Si nanowires was assembled by shear-printing[15], source and drain electrodes were defined by electron beam lithography (EBL), atomic-layer deposition was used to deposit the Al_2O_3–ZrO_2–Al_2O_3 charge-trapping structure and then a second step of EBL was used to define input gate lines. In this way, two blocks of NWFETs were fabricated, namely block 1 (Fig. 3a, left) and block 2 (Fig. 3a, right), which correspond to the unit tile of our PNNTA architecture (Fig. 2b). Dark-field optical microscopy and scanning electron microscopy images (Supplementary Fig. 3) reveal a total of 496 programmable NWFET devices laid out in two separate arrays with a total area of ~960 μm^2, where each device node consists of a single nanowire crossed by a gate line. The average area per node, ~1.9 μm^2, is relatively large in these proof-of-concept studies but does not represent a lower limit, as previous studies demonstrating close-packed nanowire assembly[17] and the scaling of charge-trapping devices[18] indicate that an area 10^3-fold smaller, ~0.0017 μm^2, is achievable.

To realize functional logic with the PNNTA tile requires uniform device characteristics among individual nanowire elements. Specifically, the deviation of the threshold voltage, V_{th}, in both the active and the inactive state must be smaller than the difference in V_{th} between the two states. We characterized the V_{th} values of 70 NWFET nodes from block 1 of the fabricated PNNTA structure in both the active and the inactive state (Fig. 3b). Notably, we found that 60 of 70 nodes (86%) in the active state had V_{th} values $\leq$2 V and that 61 of 70 nodes (87%) in the inactive state had V_{th} values $\geq$3.5 V (Fig. 3b). The high yield of NWFET devices reflects the uniformity of the Ge/Si nanowire building block[12], and controlled assembly[15] allows any defective elements to be excluded readily from the functional circuit. For the demonstration of logic



f

A	B	C_{in}	S	C_{out}
0	0	0	0 (0 V)	0 (0 V)
0	0	1	1 (2.5 V)	0 (0.6 V)
1	0	0	1 (2.4 V)	0 (0.6 V)
1	0	1	0 (0.3 V)	1 (2.0 V)
1	1	0	0 (0.3V)	1 (2.5 V)
1	1	1	1 (2.3 V)	1 (2.7 V)

Figure 3 | Fabrication, structure and logic function of a PNNTA tile. **a**, Schematic of key components of the two-block PNNTA tile, including assembled and patterned Ge/Si nanowires (cyan) with source and drain electrodes (blue), and charge-trapping trilayer gate dielectric (purple) and metal gate lines (grey). The fabricated structure consists of two blocks of NWFETs, block 1 (left) and block 2 (right). **b**, Distribution of V_{th} from 70 NWFET nodes in block 1 in the PNNTA tile. The blue and red bars represent the V_{th} values of devices in inactive and active states, respectively, with $V_{ds} = 0.5$ V. **c**, Circuit design implementing a one-bit full adder. /*A*, /*B* and /*C* denote the complementary inputs of *A*, *B* and *C*, respectively. The left- and right-hand dashed boxes outline block 1 and block 2, respectively. **d**, Voltage transfer function for *S* (red) and C_{out} (blue) from input states (0, 0, 0) to (1, 1, 1). The dashed tangent lines show the maximal voltage gains of the outputs. **e**, Output voltage levels for *S* and C_{out} for six typical input states. **f**, Truth table of full-adder logic for the six input states in **e**. The measured output voltages are shown in brackets.

circuits, we selected devices with average V_{th} values of 1.0 ± 0.4 and 3.7 ± 0.5 V for active and inactive states, respectively (Supplementary Fig. 4). Similarly, the chosen NWFET nodes in block 2 had V_{th} values of 1.4 ± 0.8 and 4.0 ± 0.3 V for active and inactive states, respectively. The distinction between V_{th} values for both states in both blocks of the PNNTA tile provide a relatively wide, ~2-V, window for circuit operation.

The two-block PNNTA tile was initially programmed to function as a full adder, an important combinational circuit in the arithmetic logic unit in modern digital computers. Figure 3c illustrates the configuration of the one-bit full-adder logic circuit comprising two blocks with the output of block 1 (Fig. 3c, left-hand box) fed into block 2 (Fig. 3c, right-hand box) as input through external wiring. The programmed active node pattern (Fig. 3c, green dots) determines the circuit function, and in this case the outputs *S* and C_{out} represent the sum and carry-out of the summation of inputs $A + B + C$, respectively, with $S = A \oplus B \oplus C$ and $C_{out} = A \cdot B + A \cdot C + B \cdot C$. The symbols '$\oplus$', '$\cdot$' and '+' represent logical XOR, AND and OR, respectively. Typical voltage transfer functions of the resulting circuit for power-supply voltage, V_{DD}, of 3.0 V (Fig. 3d) show that as the input levels of *A*, *B* and *C* are swept from logic state 0 (0 V) to logic state 1 (3.5 V), the outputs *S* and C_{out} switch from logic 0 (both 0 V) to logic 1 (2.0 and 2.7 V, respectively). From this data, the peak voltage gains of C_{out} and *S* (Fig. 3d, lines tangential to data) are found to be 10 and 4, respectively. The larger-than-unity gain and the matching of input–output voltage levels are crucial for potentially cascading the logic tiles (Supplementary Fig. 2). Further tests showed that the output of *S* and C_{out} for six typical input combinations (Fig. 3e) all had similar output ranges: 0–0.6 V for logic state 0 and 2.0–2.7 V for logic state 1. The expected and experimental results for a full adder are summarized in a truth table (Fig. 3f), which shows good consistency for this fundamental logic unit. The V_{th} value of some active NWFET nodes shifted with the 3-V source bias and precluded switching behaviour for the (*A*, *B*, *C*) = (0, 1, 0) and (0, 1, 1) inputs for a consistent input voltage range (0–3.5 V). We note that optimization of logic operations can be achieved by tuning V_{DD} and the load resistance, together with adjustment of V_{th} through the choice of top-gate metal[12]. Nonetheless, the large voltage gain and matching of input–output voltage levels described here show the potential to integrate the prototype device into large-scale integrated circuits such as a multi-bit adder in a cascade configuration.

Notably, the same PNNTA tile can be used to perform a range of distinct logic operations because we can reproducibly and independently reprogram the active and inactive nodes in both blocks (Methods and Supplementary Fig. 5). To illustrate this key point, we first reprogrammed the same tile shown in Fig. 3 to function as a full subtractor (Fig. 4a). The two outputs of the reprogrammed circuit, *D* and B_{out},

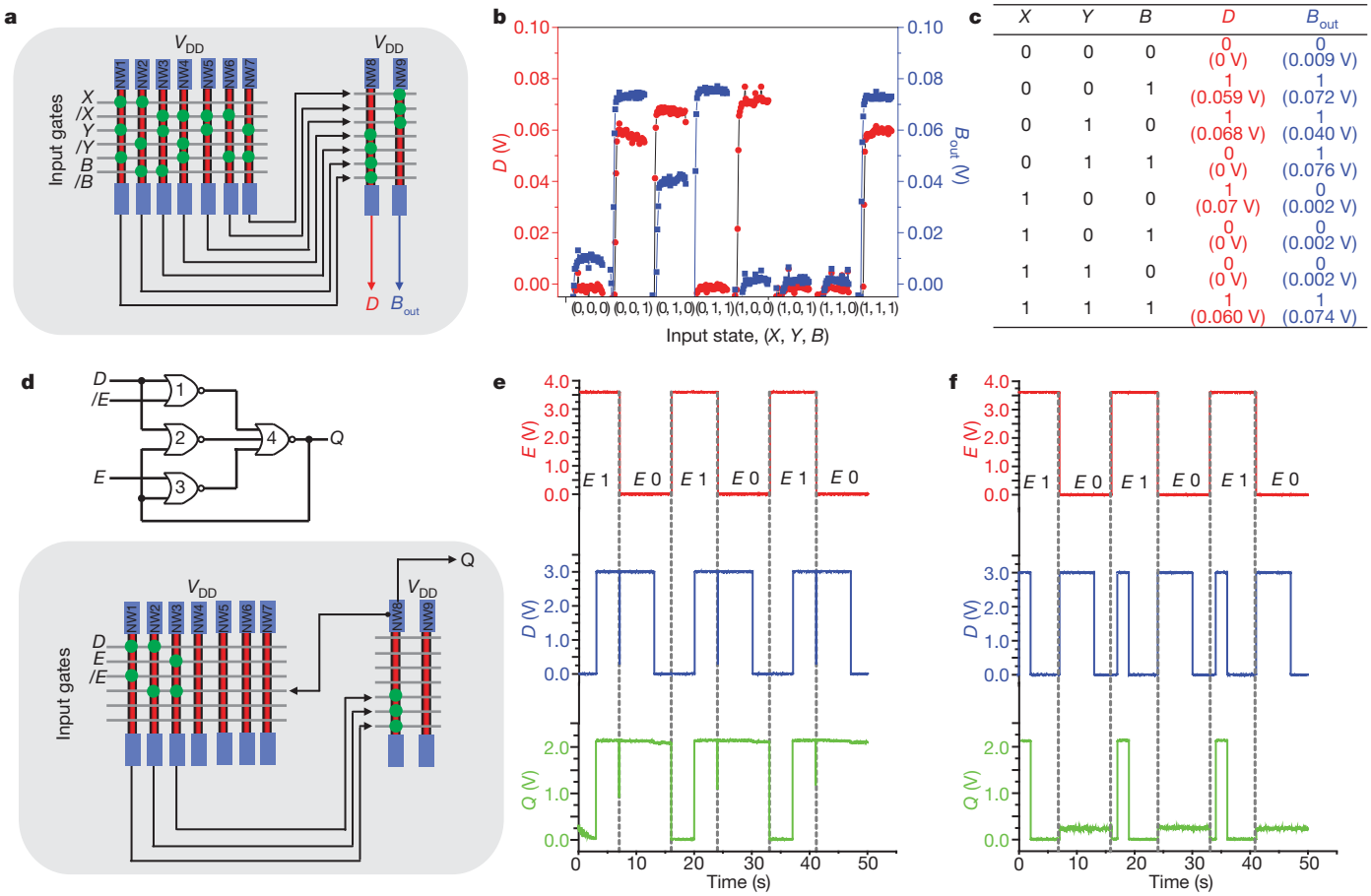


Figure 4 | Multifunctional PNNTA architecture. **a**, Schematic of a circuit implementing a full subtractor. **b**, Output of D (red) and B_{out} (blue) of the full subtractor implemented with the same PNNTA structure shown in Fig. 3 with eight input states. **c**, Truth table of the full subtractor with measured output voltages shown in brackets. **d**, Schematics of logic (upper) and circuit design (lower) of a D latch implemented with the same PNNTA tile used in **a**–**c**. **e**, **f**, Output, Q, waveforms (green) at two sets of clock (E, red) and data (D, blue) inputs.

represent the difference and borrow, respectively, of the subtraction of inputs $X-Y-B$, with $D=X\oplus Y\oplus B$ and $B_{out}=B\cdot\overline{(X\oplus Y)}+\overline{X}\cdot Y$, where $\overline{X}$ represents the logical negation of X (that is, the complementary input). Measurements of D and B_{out} for different $X-Y-B$ input combinations (Fig. 4b) show that the output voltage levels for logic state 0 (0–0.01 V) and logic state 1 (0.04–0.08 V) are well separated and represent robust states. Moreover, the truth table summarizing the expected and experimental results for the full subtractor (Fig. 4c) shows full and correct logic for this processing unit. In addition, we used the same tile to program and demonstrate multiplexer and demultiplexer circuits (Supplementary Fig. 6), showing the capability and flexibility of the PNNTA to fulfil the core functions of combinational circuit elements.

Significantly, we can also use our nanowire tile as a sequential circuit element, which represents another critical component beyond the scope of combinational elements. To do so, we mapped a D latch[19], a sequential logic circuit capable of information storage, onto the unit tile (Fig. 4d). The D-latch circuit (Fig. 4d, upper panel) is composed of four NOR gates with a positive-feedback connection between the output, Q, and inputs to NOR gates 2 and 3 (Fig. 4d, upper panel). As a consequence, Q equals input data, D, when clock, E, is in logic state 1 but retains its previous value when E is switched into logic state 0. We implemented the NOR gates in the tile using NW1–NW3 in block 1 and NW8 in block 2 (Fig. 4d, lower panel), and formed the positive feedback by connecting the output to an input gate in block 1. An important constraint on realizing the D-latch logic is that there must be a successful feedback loop (output Q of block 2 back to block 1; Fig. 4d), which requires matching of input and output voltage levels. Measurement of Q as a function of repetitive E and D pulses (Fig. 4e) shows that Q follows D when E is switched to logic 1 (3.6 V) at time points 16 and 33 s but retains its previous value when E is switched to logic 0 (0 V) at 7, 24 and 41 s, as expected for a D latch. The robustness of this sequential logic circuit was tested further by inputting a more complex data waveform (Fig. 4f), where measurements of Q demonstrated sharp logic operation by following D with high fidelity in the time intervals 16–24 and 33–41 s. Moreover, the voltage range of output, Q (0–2.2 V), closely matches that of input data, D, and clock, E.

Our nanowire logic tile has novel features in comparison with previous circuits based on bottom-up nanoscale elements[1,2,4–9]. First, the architecture enables us to enhance by a factor of at least three the complexity of nanoelectronic circuits assembled from the bottom up (56 devices of two-block, coupled logic rather than ≤16 uncoupled devices in a single block in previous work[4–6]), and correspondingly has led to circuits exceeding simple logic realized using nanowires[4–6], carbon nanotubes[7,8] and memristors[9]. Second, our circuits show a maximal voltage gain of ten, which is comparable to previous reports on simple nanowire and carbon nanotube logic devices[4–8] and represents a significant advantage over passive memristor devices[9], where gain is ≤1. Gain is crucial for signal restoration[10,11] and makes the PNNTA architecture suitable for larger-scale processors. Third, the reversible programming of individual NWFET nodes in the tile provides great versatility, as shown by the combinational and sequential circuit elements reported above. Reconfigurable logic has been realized using memristor complementary metal–oxide–semiconductor (CMOS) hybrid circuits[20], where the microscale CMOS layer is responsible for logic operation and memristors are responsible for reconfigurable signal routing. Our

architecture, however, represents the first example of a system integrating nanoscale devices that combine both logic and programmability functions. These bottom-up nanowire circuits also have limitations in comparison with conventional CMOS circuits, although projections suggest that the density, speed and power consumption can be further improved for our array architecture (Supplementary Information).

In summary, we have demonstrated a programmable and scalable architecture based on a unit logic tile consisting of two interconnected, programmable, non-volatile nanowire transistor arrays. Each NWFET node in an array can be programmed to act as an active or an inactive transistor state, and by mapping different active-node patterns into the array, combinational and sequential logic functions including full adder, full subtractor, multiplexer, demultiplexer and D-latch can be realized with the same programmable tile. Cascading this unit logic tile into linear or tree-like interconnected arrays, which will be possible given the demonstrated gain and matched input–output voltage levels of NWFET devices, provides a promising bottom-up strategy for developing increasingly complex nanoprocessors with heterogeneous building blocks[2,21]. In the near term, particularly promising for this architecture and the low-power devices it contains are simpler, tiny, application-specific nanoelectronic control processors[3]; such 'nanocontrollers' might make possible very small embedded electronic systems and new types of therapeutic device.

METHODS SUMMARY

We synthesized the Ge/Si core/shell nanowires using a nanocluster-catalysed methodology described previously[12]. Growth of the charge-trapping gate dielectric shells by atomic-layer deposition was carried out in a vacuum system (Savannah-100, Cambridge NanoTech) at 200 °C, using trimethylaluminium, tetrakis (dimethylamino)zirconium and water as precursors. The three layers were deposited without interruptions in between. Standard EBL and thermal evaporation were used to form metal electrodes (Ni for source and drain and Cr–Au for top gate). We used the focused ion beam technique to prepare a cross-sectional sample of the NWFET device, and used lubricant-assisted contact printing to prepare axially aligned Ge/Si nanowire arrays. EBL and inductively coupled plasma reactive ion etching were used to pattern the nanowires. Electrical measurements were made with a computer-controlled, analogue input–output system (National Instruments). A custom-designed 96-pin probe card (Accuprobe) was used to access devices in the PNNTA array electrically.

Received 6 August; accepted 6 December 2010.

1. Lu, W. & Lieber, C. M. Nanoelectronics from the bottom up. *Nature Mater.* **6,** 841–850 (2007).
2. Lu, W., Xie, P. & Lieber, C. M. Nanowire transistor performance limits and applications. *IEEE Trans. Electron. Dev.* **55,** 2859–2876 (2008).
3. Das, S. *et al.* Designs for ultra-tiny, special-purpose nanoelectronic circuits. *IEEE Trans. Circuits Syst. Regul. Pap.* **54,** 2528–2540 (2007).
4. Cui, Y. & Lieber, C. M. Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *Science* **291,** 851–853 (2001).
5. Huang, Y. *et al.* Logic gates and computation from assembled nanowire building blocks. *Science* **294,** 1313–1317 (2001).
6. Zhong, Z. H., Wang, D. L., Cui, Y., Bockrath, M. W. & Lieber, C. M. Nanowire crossbar arrays as address decoders for integrated nanosystems. *Science* **302,** 1377–1379 (2003).
7. Bachtold, A., Hadley, P., Nakanishi, T. & Dekker, C. Logic circuits with carbon nanotube transistors. *Science* **294,** 1317–1320 (2001).
8. Javey, A. *et al.* High-κ dielectrics for advanced carbon-nanotube transistors and logic gates. *Nature Mater.* **1,** 241–246 (2002).
9. Borghetti, J. *et al.* 'Memristive' switches enable 'stateful' logic operations via material implication. *Nature* **464,** 873–876 (2010).
10. DeHon, A. Array-based architecture for FET-based, nanoscale electronics. *IEEE Trans. Nanotechnol.* **2,** 23–32 (2003).
11. Das, S., Rose, G. S., Ziegler, M. M., Picconatto, C. A. & Ellenbogen, J. C. Architectures and simulations for nanoprocessor systems integrated on the molecular scale. *Lect. Notes Phys.* **680,** 479–513 (2005).
12. Xiang, J. *et al.* Ge/Si nanowire heterostructures as high-performance field-effect transistors. *Nature* **441,** 489–493 (2006).
13. Liu, J., Wang, Q., Long, S. B., Zhang, M. H. & Liu, M. A metal/Al_2O_3/ZrO_2/SiO_2/Si (MAZOS) structure for high-performance non-volatile memory application. *Semicond. Sci. Technol.* **25,** 055013 (2010).
14. Sze, S. M. *Physics of Semiconductor Devices* 438–445 (Wiley, 1981).
15. Javey, A., Nam, S., Friedman, R. S., Yan, H. & Lieber, C. M. Layer-by-layer assembly of nanowires for three-dimensional, multifunctional electronics. *Nano Lett.* **7,** 773–777 (2007).
16. Snider, G., Kuekes, P. & Williams, R. S. CMOS-like logic in defective, nanoscale crossbars. *Nanotechnology* **15,** 881–891 (2004).
17. Whang, D., Jin, S., Wu, Y. & Lieber, C. M. Large-scale hierarchical organization of nanowire arrays for integrated nanosystems. *Nano Lett.* **3,** 1255–1259 (2003).
18. Sakamoto, W. *et al.* in *Proc. Electronic Devices Meeting 2009*, doi:10.1109/IEDM.2009.5424211 (IEEE, 2009).
19. Sedra, A. S. & Smith, K. C. *Microelectronics Circuits* 1014–1021 (Oxford Univ. Press, 2004).
20. Xia, Q. F. *et al.* Memristor-CMOS hybrid integrated circuits for reconfigurable logic. *Nano Lett.* **9,** 3640–3645 (2009).
21. Nam, S., Jiang, X. C., Xiong, Q. H., Ham, D. & Lieber, C. M. Vertically integrated, three-dimensional nanowire complementary metal-oxide-semiconductor circuits. *Proc. Natl Acad. Sci. USA* **16,** 21035–21038 (2009).

Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

Acknowledgements We thank D. Bell and N. Antoniou for transmission electron microscopy sample preparation and imaging, Q. Qing for assistance with electrical measurements and J. L. Huang, X. Duan and X. Jiang for helpful discussions. C.M.L. acknowledges support from a National Security Science and Engineering Faculty Fellow award and a contract from the MITRE Corporation. S.D., J.F.K. and J.C.E. acknowledge support by the US government's Nano-Enabled Technology Initiative and the MITRE Innovation Program.

Author Contributions C.M.L., J.C.E., S.D., H.Y., H.S.C. and S.N. designed the experiments. H.Y., H.S.C., S.N., Y.H. and J.F.K. performed the experiments. S.D. performed simulations. H.Y., H.S.C., S.N., S.D., J.F.K., J.C.E. and C.M.L. analysed the data and wrote the paper. All authors discussed the results and commented on the manuscript.

Author Information Reprints and permissions information is available at www.nature.com/reprints. The authors declare no competing financial interests. Readers are welcome to comment on the online version of this article at www.nature.com/nature. Correspondence and requests for materials should be addressed to S.D. (sdas@mitre.org) or C.M.L. (cml@cmliris.harvard.edu).