LETTERS

Ge/Si nanowire heterostructures as high-performance field-effect transistors

Jie Xiang[1]*, Wei Lu[1]*, Yongjie Hu[1], Yue Wu[1], Hao Yan[1] & Charles M. Lieber[1,2]

Semiconducting carbon nanotubes[1,2] and nanowires[3] are potential alternatives to planar metal-oxide-semiconductor field-effect transistors (MOSFETs)[4] owing, for example, to their unique electronic structure and reduced carrier scattering caused by one-dimensional quantum confinement effects[1,5]. Studies have demonstrated long carrier mean free paths at room temperature in both carbon nanotubes[1,6] and Ge/Si core/shell nanowires[7]. In the case of carbon nanotube FETs, devices have been fabricated that work close to the ballistic limit[8]. Applications of high-performance carbon nanotube FETs have been hindered, however, by difficulties in producing uniform semiconducting nanotubes, a factor not limiting nanowires, which have been prepared with reproducible electronic properties in high yield as required for large-scale integrated systems[3,9,10]. Yet whether nanowire field-effect transistors (NWFETs) can indeed outperform their planar counterparts is still unclear[4]. Here we report studies on Ge/Si core/shell nanowire heterostructures configured as FETs using high-κ dielectrics in a top-gate geometry. The clean one-dimensional hole-gas in the Ge/Si nanowire heterostructures[7] and enhanced gate coupling with high-κ dielectrics give high-performance FETs values of the scaled transconductance ($3.3\,\mathrm{mS\,\mu m^{-1}}$) and on-current ($2.1\,\mathrm{mA\,\mu m^{-1}}$) that are three to four times greater than state-of-the-art MOSFETs and are the highest obtained on NWFETs. Furthermore, comparison of the intrinsic switching delay, $\tau = CV/I$, which represents a key metric for device applications[4,11], shows that the performance of Ge/Si NWFETs is comparable to similar length carbon nanotube FETs and substantially exceeds the length-dependent scaling of planar silicon MOSFETs.

Silicon[9,10,12] and germanium[13,14] nanowires have been the focus of recent studies of one-dimensional (1D) FETs. However, metal contacts to single-component nanowires generally produce Schottky barriers that limit device performance[15], and moreover, scattering from charged dopants can also reduce the intrinsic mobility of these nanowire devices[15]. In contrast, we have recently demonstrated transparent contacts and low-bias ballistic transport[7] in undoped Ge/Si core/shell nanowire heterostructures (Fig. 1a, b), with an estimated scattering mean free path of ~500 nm. The 1D sub-band spacing in the typical 15-nm core Ge/Si nanowires determined through both experimental measurements and theoretical calculations[7] is ~25 meV, and thus at room temperature several sub-bands may participate in NWFET transport. While the Ge/Si nanowire devices will not be strictly 1D, the limited number of conduction channels and clean material structure can benefit performance through, for example, a reduction in scattering. To explore the potential of Ge/Si nanowire heterostructures as high-performance FETs we have fabricated (see Methods) devices using thin HfO_2 or ZrO_2 high-κ gate dielectrics and metal top gate electrodes (Fig. 1c, d). Cross-sectional transmission electron microscopy (TEM) images (Fig. 1e) show that both the high-κ and metal top gate conform to the approximately circular cross-section of the nanowire, and also verify the Ge/Si core/shell structure. The conformal top gate structure approaches an ideal cylindrical gate geometry, and together with the high-κ dielectrics produces a much more efficient gate response than previous studies using lower-κ SiO_2 dielectric and planar back gates[9,12,16].

Typical output and transfer characteristics recorded from a Ge/Si device fabricated in this way with a channel length, $L = 1\,\mu m$ and a total diameter of 18 nm (device A) are shown in Fig. 2a, b. The family of I_d–V_{ds} curves (Fig. 2a) show that the drain current I_d first increases then saturates with increasingly negative drain voltage, similar to a conventional long channel MOSFET[11]. These data also show that I_d increases as the gate voltage V_g decreases from 1 to −2 V, and thus that the device is a *p*-type depletion-mode FET. This *p*-type FET behaviour is expected from the band diagram in Fig. 1b, where the Fermi level lies below the Ge valence band edge in the absence of a gate. The I_d–V_g transfer curve recorded for the drain bias voltage

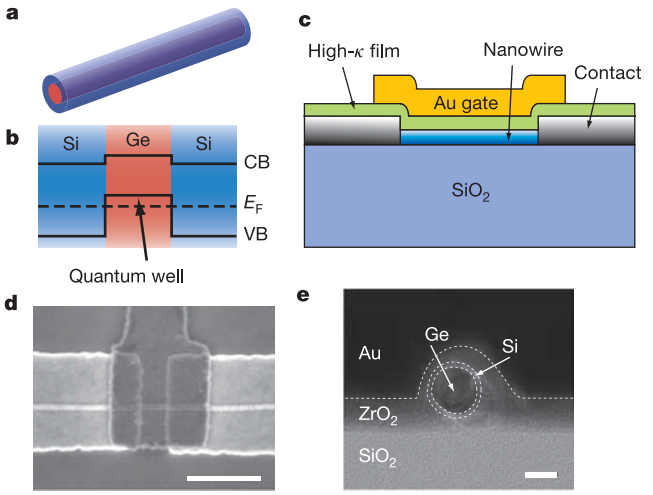

Figure 1 | Ge/Si core/shell NWFET. a, Schematic of a Ge/Si core/shell nanowire. **b**, Cross-sectional diagram showing the formation of hole-gas in the Ge quantum well confined by the epitaxial Si shell, where CB is the conduction band and VB is the valence band. The dashed line indicates the Fermi level, E_F. The valence band offset of ~500 meV between Ge and Si serves as a confinement potential to the hole-gas as discussed previously[7]. **c**, Schematic of the NWFET device with high-κ dielectric layer and Au top gate. **d**, Top-view SEM image of a typical device. The Au top gate overlaps with the Ni source/drain electrodes to ensure full coverage of the channel. Scale bar, 500 nm. **e**, Cross-sectional TEM image of a device prepared using 7 nm ZrO_2 dielectric. Dotted lines are guides to the eye showing boundaries between different materials denoted in the image. The nanowire is tilted off the imaging axis. Scale bar, 10 nm.

[1]Department of Chemistry and Chemical Biology, [2]Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts 02138, USA.
*These authors contributed equally to this work.

$V_{ds} = -1$ V (Fig. 2b) demonstrates that the NWFET has a peak transconductance, $g_m = dI_d/dV_g$, of 26 μS. In addition, the device exhibits a maximum drain current $I_{d(max)}$ of 35 μA at $V_g = -2$ V. We note these values of g_m and $I_{d(max)}$ substantially exceed the best performance reported to date in single semiconductor NWFETs[12,14].

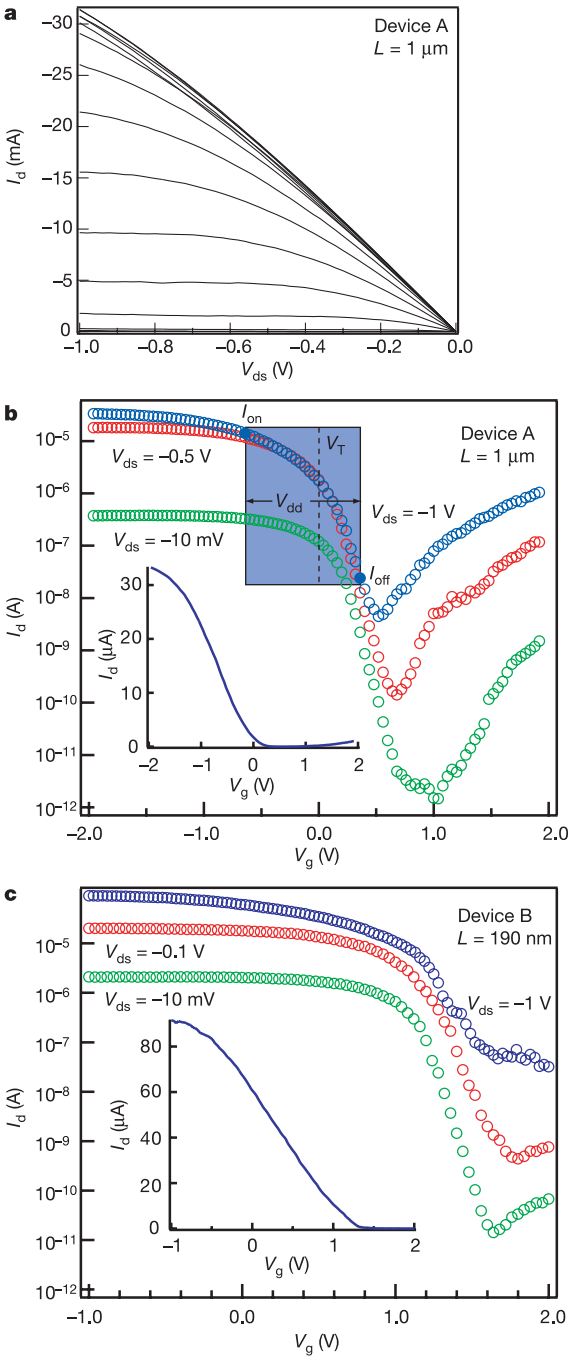

Figure 2 | Characteristics of high-performance Ge/Si NWFET. a, I_d–V_{ds} data for device A ($L = 1$ μm, 4 nm HfO_2 dielectric) with $V_g = -2$ to 2 V in 0.25 V steps from top to bottom. **b**, I_d–V_g for device A with blue, red, and green data points corresponding to V_{ds} values of −1, −0.5 and −0.01 V, respectively. The leakage current through the gate electrode (I_g) is $<10^{-10}$ A, which excludes I_g as source of increase in I_d at $V_g > \sim 0.5$ V. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V. The blue-shaded area defines the 1 V gate voltage window described in the text, where V_T was determined from the intercept of the tangent of maximum slope (linear transconductance) region of the I_d–V_g curve[11]. **c**, I_d–V_g data for device B ($L = 190$ nm, 4 nm HfO_2 dielectric) with blue, red and green data points corresponding to V_{ds} values of −1, −0.1 and −0.01 V, respectively. Inset, linear scale plot of I_d versus V_g measured at $V_{ds} = -1$ V.

The on current I_{on} for a FET device is usually determined at $V_g = V_{ds} = V_{dd}$, where V_{dd} is the power supply voltage and equals 1 V in our case. Following conventions in planar devices, we define on and off currents as the values measured at $V_{g(on)} = V_T - 0.7V_{dd}$ and $V_{g(off)} = V_T + 0.3V_{dd}$, so that 30% of the V_g swing above the threshold voltage V_T is applied to turn the device off, while the remaining 70% sets the operation range of the on state (Fig. 2b). Similar methods have been proposed in benchmarking carbon nanotube FET devices[4,17]. From Fig. 2b, we obtain $I_{on} = 14$ μA for this 1-μm-long device. Significantly, the scaled values of g_m and I_{on}, 1.4 mS μm^{-1} and 0.78 mA μm^{-1}, using the total nanowire diameter as the device width, already exceeds the values of 0.8 mS μm^{-1} and 0.71 mA μm^{-1} recently reported in much shorter, sub-100-nm silicon *p*-MOSFETs employing high-κ dielectrics[18].

In addition, we have prepared and studied a large number of Ge/Si NWFET devices with L varying from 1 μm to 190 nm; essentially all of these devices exhibited high-performance behaviour and testify to the reproducibility of both the Ge/Si nanowires and contacts to this material. Representative data obtained from a $L = 190$ nm device (device B), which should exhibit larger g_m and I_d values owing to reduced channel resistance, are shown in Fig. 2c. These data yield $g_m = 60$ μS, $I_{on} = 37$ μA ($V_{dd} = 1$ V), and $I_{d(max)} = 91$ μA, and correspond to scaled values of g_m and I_{on} of 3.3 mS μm^{-1} and 2.1 mA μm^{-1}, respectively. Notably, these values are more than twice that achieved in the longer channel device and are 3–4 times greater than state-of-the-art Si *p*-MOSFETs[18]. The geometric gate capacitance per unit area in our NWFETs, 44 fF μm^{-2} (Methods), is only 29% larger than the 34 fF μm^{-2} in these Si *p*-MOSFETs[18]. Therefore the large gain in g_m and I_{on} cannot be accounted for by an increase in gate capacitance alone. Moreover, the hole mobility for this Ge/Si NWFET, 730 cm^2 V^{-1} s^{-1}, extracted at the linear region ($|V_{ds}| = 10$ mV) from the peak $g_m = 3$ μS at $|V_g - V_T| = 0.13$ V using the charge control model, represents an improvement of more than a factor of ten over that of the Si *p*-MOSFET with HfO_2 gate dielectric (50–60 cm^2 V^{-1} s^{-1})[18], and also is more than twice the reported low-field mobility of Ge and strained SiGe heterostructure PMOS devices[19,20]. Improved mobility is observed for NWFETs with channel lengths from 0.19 to 1 μm (Supplementary Fig. S1), with an average of 640 cm^2 V^{-1} s^{-1}. These improvements over planar device structures thus verify the performance benefit due to the quasi-1D transport in clean Ge/Si heterostructure nanowires.

The subthreshold region of the I_d–V_g data was also analysed and yields values of the slope, $S = -[d(\log_{10}I_d)/dV_g]^{-1}$, of 105 and 100 mV per decade for the $L = 1$ μm and 190 nm NWFETs, respectively, for $V_{ds} = -1$ V (Fig. 2b, c). Similar values of S were obtained from I_d–V_g data recorded on both devices using V_{ds} from −0.01 to −1 V, which indicate the absence of significant short-channel effects[11] for devices down to at least $L = 190$ nm and excellent V_g control of the channel potential over the competing effect of drain-induced barrier lowering at larger biases[11].

In general, an FET with a small S is essential for modern logic circuits as it reduces the off state current and minimizes static power dissipation. The value of S can be estimated[11] by $2.3k_BT/e\alpha$, where T is temperature and α is the gate-coupling factor, which yields a room temperature minimum ($\alpha = 1$) of 60 mV per decade. The values of S determined for the $L = 1$ μm and 190 nm Ge/Si NWFETs are superior to the best value (140 mV per decade) reported previously[9] for NWFETs but still larger than the theoretical minimum. The non-ideal gate coupling ($\alpha < 1$), which yields this larger S value, is probably due to a finite trap state density at the nanowire/high-κ interface[21]. Optimization of the high-κ deposition process during fabrication or growth of a cylindrical high-κ shell on the Ge/Si nanowire before fabrication should yield improved interface quality and enable us to approach ideal subthreshold behaviour in the future in these NWFETs.

An important benchmark of transistor performance is the intrinsic delay, $\tau = CV/I$, where C is the gate capacitance, $V = V_{dd}$, and I is on current I_{on}. As defined, τ represents the fundamental RC (where R is the device resistance and C is the capacitance) delay of the device and provides a frequency limit for transistor operation that is relatively insensitive to gate dielectrics and device width, and thus represents a good parameter for comparing different types of devices[11]. The calculated intrinsic delays are 57 and 4 ps for devices A and B in Fig. 2, respectively, where C was determined by numerical simulation (Methods). A summary of the results from seven Ge/Si NWFETs versus L and the corresponding scaling for Si MOSFETs (Fig. 3a) highlights several key points. First, the data show clear speed advantage at a given L for the Ge/Si NWFETs versus Si p-MOSFETs. For example, the intrinsic delay for a 190 nm Si planar device is larger than 10 ps, about three times longer than our device B. Second, the delay time for the 190 nm Ge/Si device is about the same as that of similar-length CNTFET devices[4]. Last, length scaling of τ is more favourable for our Ge/Si NWFETs than Si MOSFETs (that is, slope of ~1.5 versus ~1.1). We attribute this important difference to a suppression of scattering in the quasi-1D quantum confined Ge/Si nanowires versus MOSFETs[22], although additional studies will be needed to support this idea.

To capture the off state leakage current property, we used a method described by ref. 17 and studied the CV/I_{on} versus I_{on}/I_{off} ratio. Here we assume full control of the threshold voltage, allowing a window of $V_{g(on)}$–$V_{g(off)} = V_{dd} = 1$ V to move along the V_g axis and define a pair of I_{on} and I_{off} value from the I_d–V_g data plot. The CV/I_{on} versus I_{on}/I_{off} data for devices A and B (Fig. 3b) shows the trade-off between high speed and small leakage. The smallest τ is observed at the largest I_{on}, although this corresponds to a minimum on/off ratio. As the on/off ratio increases τ also increases[4], until the on/off ratio reaches a maximum limited by ambipolar conduction (see below). The arrows correspond to the intrinsic delay values obtained from the 70–30% criteria used to define I_{on} in the benchmark plot in Fig. 3a, and show that the I_{on}/I_{off} ratios for the A and B devices are 100 and 580, respectively. On/off ratios for the rest of the devices in Fig. 3a all lie within this range. The on/off ratio is expected to reach 10^4–10^5 as the subthreshold slope is improved to the ideal value of 60 mV per decade. Studies of strained SiGe planar devices show that subthreshold slopes of 66–70 mV per decade are achievable[20], although we note that the on/off ratio of 10^2 may already meet a lower practical limit for certain high-performance applications[23].

The above Ge/Si NWFETs are depletion-mode devices with threshold voltages $V_T > 0$, and require $V_g > V_T$ to be turned off. However, enhancement-mode FETs with $V_T < 0$, which are off for $V_g = 0$, are technologically more desirable because they consume less static power. In addition and as discussed above, obtaining the optimal device operation depends critically on the full control of the threshold voltage. We have exploited the top gated structure (Fig. 1c) to tune V_T through variations in the gate metal work function. Comparison of I_d–V_g data recorded using Au and Al metal gates (Fig. 4a) clearly shows a change from depletion mode, $V_T = +0.65$ V, to enhancement mode $V_T = -0.65$ V, while other key device parameters remain the same. Measurements made on 68 NWFETs yield average threshold values of 0.53 ± 0.17 and

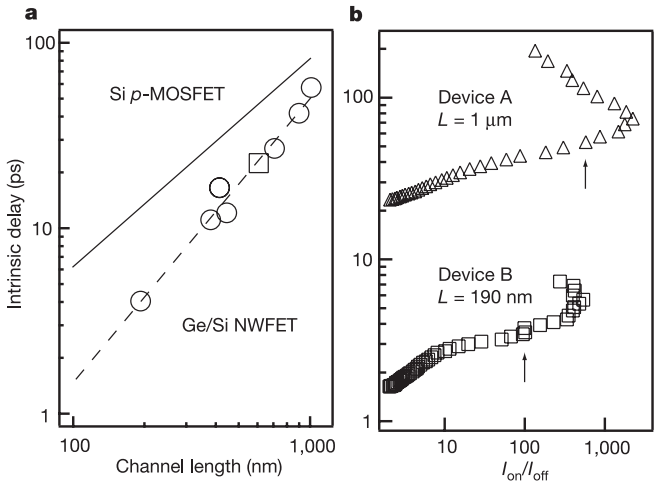

Figure 3 | Benchmark and comparison of Ge/Si FETs. **a**, Intrinsic delay τ versus channel length for seven different Ge/Si nanowire devices with HfO_2 dielectric (open circle) and ZrO_2 dielectric (open square). Data for devices A and B are included. The I_{on} values were measured at $V_{g(on)} = V_T - 0.7V_{dd}$, as discussed in the text. The dashed line is a fit to the data points while solid line is the Si p-MOSFET results from ref. 4. **b**, Intrinsic delay versus on/off ratio for the two devices in Fig. 2. Arrows indicate the values of intrinsic delay used in **a**.

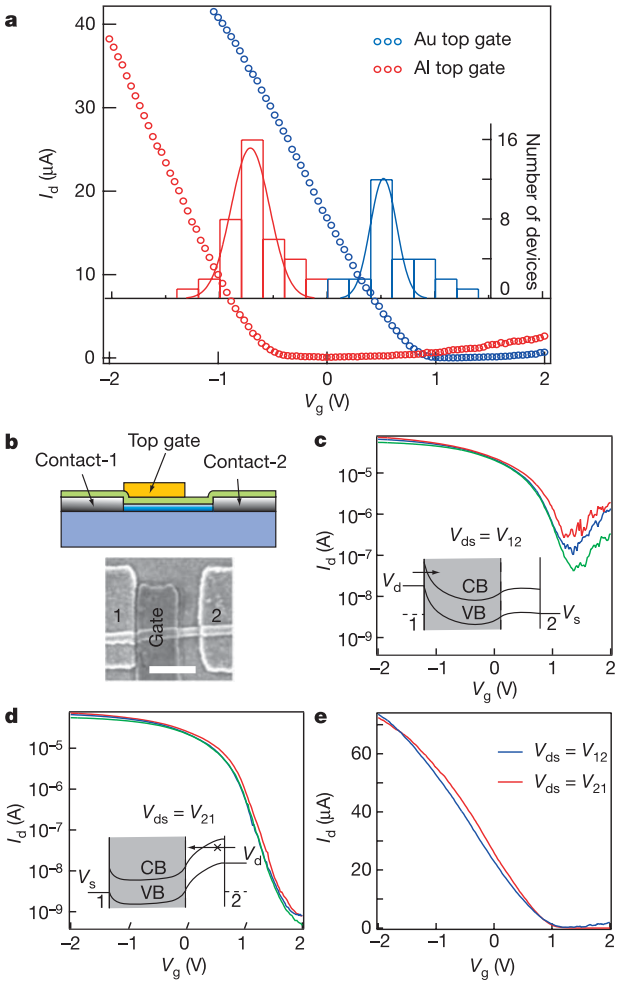

Figure 4 | Control of threshold voltage and ambipolar conduction through device design. **a**, I_d–V_g curves for two $L = 300$ nm devices with Au (blue) and Al (red) top gate electrodes ($V_{ds} = -1$ V). Inset shows histogram of V_T with the same V_g axis for a total of 68 $L = 300$ nm devices with Au (blue) and Al (red) top gates. Solid lines correspond to gaussian fits to the two distributions. **b**, Schematic and SEM image of the asymmetrical gate structure designed to suppress ambipolar conduction. Scale bar, 300 nm. **c**, I_d–V_g of partially gated device with ambipolar conduction; bias was applied to contact 1 ($V_{ds} = V_{12}$). Inset, schematic of band bending in the NWFET at finite bias. Arrow denotes electron injection at the drain contact. **d**, I_d–V_g for $V_{ds} = V_{21}$. Inset, schematic of band bending with electron injection denoted by arrow. The red, blue and green curves in **c** and **d** correspond to V_{ds} values of −1, −0.8 and −0.6 V, respectively. **e**, Linear scale I_d–V_g ($V_{ds} = -1$ V) for the devices in **c** and **d**. The two devices have the same peak $g_m = 35$ μS and $I_{d(max)} = 73$ μA.

-0.72 ± 0.25 V for Au and Al top gates, respectively, and thus demonstrate the reproducibility of this effect in our high-performance Ge/Si NWFETs. The V_T shift of 1.25 V corresponds approximately to the work function difference between Au ($\Phi_{Au} = 5.31$–5.47 eV) and Al ($\Phi_{Al} = 4.28$ eV) with small deviations attributable to metal/dielectric interface states[24]. More generally, these results indicate that it will be possible to tune V_T for specific applications simply through a choice of top gate metal with specific work function in fabrication.

The Ge/Si NWFETs also exhibit an increase in I_d when V_g is increased to larger positive values (for example, Fig. 2) owing to conduction by electron carriers (versus holes). Similar ambipolar conduction has been observed in high-performance CNTFETs with metal contacts[4,25,26], and is deleterious for applications since it reduces the window of operation and increases the minimum off-state current. To address this issue we characterized devices with asymmetrical partial gates (Fig. 4b). Data recorded from a NWFET with bias voltage applied to contact 1 (proximal to the gate) and holding contact 2 at ground (Fig. 4c), $V_{ds} = V_{12}$, show ambipolar conduction like the fully gated device in Fig. 2. Significantly, switching the source and drain electrodes ($V_{ds} = V_{21}$) dramatically suppresses the ambipolar current from 300 to 0.8 nA at $V_{ds} = -1$ V (Fig. 4d). These results can be explained by the corresponding band diagrams (insets, Fig. 4c, d). In the first case, electron injection at the drain increases with increasing V_g and ultimately dominates the current, while in the second, the ungated region near contact 2 acts as a thick barrier to electron transport and suppresses electron current even at large downward bending of the conduction band.

Importantly, the reduction in ambipolar current using this device structure does not limit other key NWFET characteristics. The on state conductance and transconductance (Fig. 4e) show no degradation compared to fully gated devices with similar dimensions (for example, Fig. 4a), and S (Fig. 4d) shows little V_{ds} dependence, indicating excellent gate control[11]. These observations contrast with experiments on CNTFETs with similar gate structures[27], which may have been limited by the presence of Schottky barriers at the CNT contacts. Such limitations do not exist for Ge/Si NWFETs, which do not have contact barriers[7], and thus the asymmetrical gate structure can yield unipolar NWFETs without sacrificing performance.

In summary, we have demonstrated top-gated Ge/Si NWFET heterostructures with high-κ dielectrics that exhibit scaled transconductance and on-current values of 3.3 mS μm^{-1} and 2.1 mA μm^{-1}, respectively, which are three to four times greater than those for state-of-the-art MOSFETs. In addition, the Ge/Si NWFET hole mobility, 730 $cm^2 V^{-1} s^{-1}$, is more than a factor of ten greater than the Si p-MOSFET with HfO_2 gate dielectric[18] and more than twice that of Ge and strained SiGe heterostructure PMOS devices[19,20]. These values, together with the demonstrated control over threshold voltage and ambipolar behaviour, suggest substantial promise of Ge/Si NWFETs, although further performance improvements at the single device level should also be possible through optimization of gate coupling and size scaling[28]. Looking to the future, the ability to prepare high-performance Ge/Si NWFETs in close to 100% yield, which represents a distinct advantage over similar performance CNTs, and assemble nanowires *en masse* in addressable arrays[9] could open up advances and applications in several areas, including high-frequency electronics on plastic and glass substrates[10], higher-sensitivity nanosensors[29], and possibly extending the roadmap for high-performance logic.

METHODS

Fabrication and measurement of Ge/Si NWFET devices. The growth of epitaxial core/shell Ge/Si nanowires and fabrication of Ni-contacted NWFETs are described elsewhere[7]. Nanowires have an average core diameter of 14.6 nm and Si shell thickness of 1.7 nm, and normally exhibit <110> growth direction. A thin high-κ dielectric film was deposited on the devices using the atomic layer deposition (ALD) process. 30 cycles for HfO_2 deposition and 50 cycles for ZrO_2 were used at 110 °C with each cycle consisting of 1 s water vapour pulse, 5 s N_2 purge, 3 s precursor, and 5 s N_2 purge. Tetrakis(dimethylamino) hafnium [$Hf(N(CH_3)_2)_4$], and tetrakis(dimethylamino) zirconium were used as precursors. Electron beam lithography was used to define the top gate, followed by thermal evaporation of either Cr/Au (5 nm/50 nm) or Al (50 nm). The devices were measured at room temperature in vacuum ($P < 10^{-4}$ torr) with a probe station (TTP-4, Desert Cryogenics).

Cross-sectional TEM sample preparation. Dry-transfer from the growth substrate was used to deposit aligned nanowire arrays with inter-nanowire spacings of several micrometres on a Si/SiO_2 wafer. The wafer was then coated with a thin film of ZrO_2 high-κ dielectric and Au metal as described above. Cross-sectional TEM samples were prepared by cutting the wafer into thin slices, followed by mechanical polishing and further thinning by ion milling. TEM images were taken by a JEOL 2010F high-resolution microscope.

Calculation of mobility and intrinsic delay *CV/I*. The gate capacitance, C, was calculated using numerical simulations on nanowire devices with a Ge core diameter of 14.6 nm and a Si shell thickness of 1.7 nm; these parameters were determined for devices using cross-sectional TEM measurements. The thickness for HfO_2 ($\kappa = 23$) and ZrO_2 ($\kappa = 20$) are 4 and 7 nm, respectively. Assuming the top gate conformally covers the top half of the nanowire as indicated by the cross-sectional TEM image, we obtained the gate capacitances per unit length of $C_L = 800$ aF μm^{-1} (HfO_2) and 580 aF μm^{-1} (ZrO_2) from two-dimensional electrostatic simulations (Quickfield, Tera Analysis, Denmark). When scaled using the total diameter of the nanowire, we obtained gate capacitances per unit area of 44 and 32 fF μm^{-2} for the HfO_2 and ZrO_2 dielectrics used, respectively. We note that the calculation tends to overestimate the gate coupling capacitance because it does not include the effect of quantum capacitance from the finite density of states in the 1D Ge channel[30], and does not consider the formation of interfacial silicon oxide layer that tends to reduce the κ value. Mobility is calculated from low-bias g_m based on the charge control model: $\mu = \frac{g_m}{V_{ds}} \cdot \frac{L^2}{C}$, where L is device gate length. Supplementary Fig. S1 shows a linear relationship between the inverse transconductance and the channel length for three different devices, consistent with this model. For the intrinsic delay CV/I_{on}, $V = V_{dd} = 1$ V is the power supply voltage for both the V_g swing and saturation bias.

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