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Sub-100 Nanometer Channel Length Ge/Si Nanowire Transistors with Potential for 2 THz Switching Speed

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ABSTRACT

Ge/Si core/shell nanowires (NWs) are attractive and flexible building blocks for nanoelectronics ranging from field-effect transistors (FETs) to low-temperature quantum devices. Here we report the first studies of the size-dependent performance limits of Ge/Si NWFETs in the sub-100 nm channel length regime. Metallic nanoscale electrical contacts were made and used to define sub-100 nm Ge/Si channels by controlled solid-state conversion of Ge/Si NWs to $NiSi_xGe_y$ alloys. Electrical transport measurements and modeling studies demonstrate that the nanoscale metallic contacts overcome deleterious short-channel effects present in lithographically defined sub-100 nm channels. Data acquired on 70 and 40 nm channel length Ge/Si NWFETs with a drain−source bias of 0.5 V yield transconductance values of 78 and 91 μS, respectively, and maximum on-currents of 121 and 152 μA. The scaled transconductance and on-current values for a gate and bias voltage window of 0.5 V were 6.2 mS/μm and 2.1 mA/μm, respectively, for the 40 nm device and exceed the best reported values for planar Si and NW p-type FETs. In addition, analysis of the intrinsic switching delay shows that terahertz intrinsic operation speed is possible when channel length is reduced to 70 nm and that an intrinsic delay of 0.5 ps is achievable in our 40 nm device. Comparison of the experimental data with simulations based on a semiclassical, ballistic transport model suggests that these sub-100 nm Ge/Si NWFETs with integrated high-κ gate dielectric operate near the ballistic limit.

There exist a growing number of challenges[1] associated with continuation of the remarkable scaling in performance and density of planar FETs achieved in the semiconductor industry over the past several decades due to physical and technical limitations of current device structures.[2,3] To overcome these issues, many researchers have been exploring chemically synthesized nanostructures, including semiconducting NWs and carbon nanotubes (CNTs). Researchers have shown that NW and CNT building blocks can be configured as p-type and n-type FETs and also used to "build" small logic circuits.[4–6] Moreover, there have been efforts addressing fundamental performance limits of CNT and NW FETs. CNT FETs with sub-100 nm channel lengths and performance exceeding p-type planar metal-oxide-semiconductor FETs (MOSFETs) have been reported,[7a–c] and analysis of data has shown that these devices operate near the ballistic limit.[7d,e] These advances demonstrate the promise of CNT FETs, although development of CNT FET-based nanoelectronics will require advances in the production of uniform, semiconducting material versus mixtures of metallic and semiconductor CNTs.

Semiconductor NWs can be prepared with uniform and rationally controlled electronic properties in high yield[4,5] and thus offer substantial potential for exploring bottom-up approaches to nanoelectronic circuits, quantum devices, nanophotonics, and biological detectors.[8] An interesting example of our ability to "design" nanostructure electronic properties comes from emerging studies of Ge/Si core/shell NW heterostructures.[9–11] In particular, the structure of undoped Ge/Si NWs readily yields transparent contacts to a confined Ge conduction channel with a low-bias voltage mean-free-path on the order of hundreds of nanometers at room temperature,[11a] characteristics that are attractive for high-performance FETs[10] and low-temperature quantum devices.[11b,c] Indeed, previous studies of Ge/Si NWFETs with channel lengths from 1 to 0.2 μm have shown scaled transconductance and on-current values that exceed substantially the performance of state-of-the-art Si MOSFETs.[10,12]

Critical tests of the true performance limits of Ge/Si NWFETs and comparison of these limits to other FET

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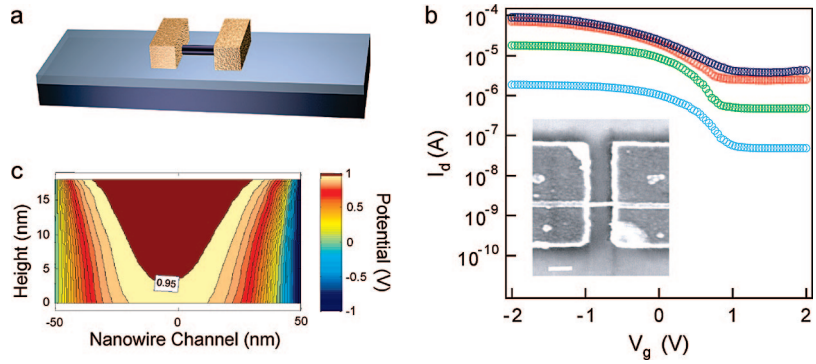

Figure 1. (a) Schematic of Ge/Si NW (dark blue) contacted with lithographically defined metal electrodes (gold). (b) Typical transport data from a 100 nm channel device with $V_{ds} = -10$ mV and -0.1, -0.5, and -0.8 V, for cyan, green, red, and dark blue, respectively. Inset: scanning electron microscopy (SEM) image of a representative device. Scale bar is 100 nm. (c) Cross-section plot of the electrostatic potential from a 3D simulation at the off-state.[15] The plot is along the 100 nm NW channel (from -50 to 50 nm).

systems require studies of device scaling in the sub-100 nm channel length regime. A straightforward approach for testing this regime involves fabrication of NWFETs with ≤100 nm channels defined directly by lithography, as illustrated in Figure 1a.[13] The Ge/Si core/shell NWs used in these studies were synthesized by a two-step chemical vapor deposition process described previously.[11a] Top-gated devices were fabricated by electron-beam lithography.[13] Typical transport data recorded on a 100 nm channel length device (Figure 1b) shows several important features. First, a large on-state current of ~0.1 mA was observed with a drain−source bias voltage (V_{ds}) of −0.8 V. The large drive current is consistent with excellent transport characteristics of Ge/Si NWs and the small channel length. Second, the off-current of 4 μA is quite large and limits the maximum on/off ratio to only 25. Third, even as V_{ds} is reduced further to 10 mV (Figure 1b), the off-state current, 50 nA, remains sizable.

Qualitatively, the large off-state current and small on/off ratio can be attributed to the electrostatic screening of gate coupling from the large lithography-defined contact electrodes[14] because the gate dielectric thickness, 4 nm, is much less than the channel length. To assess the validity of this suggestion, we performed 3-dimensional (3D) finite element simulations of the electrostatics of a NW device at the off-state.[15] Figure 1c shows a 2D cross-section plot of the electrostatic potential distribution inside a 100 nm Ge/Si NW channel along the axial direction with $V_{ds} = -1$ V and top-gate bias $V_g = +1$ V. In the middle of the channel, the electrostatic potential is reduced to <0.95 V, smaller than the applied gate potential due to electric field lines terminating on the source/drain (S/D) electrodes. These results show that large S/D contact electrodes will screen the electrical field from the gate in short channels and thus limit gate voltage control at the off-state.

One approach to overcoming the unfavorable electrostatics would be to shrink substantially the size of the S/D electrodes.[14] We have evaluated this approach using 3D simulations described above[15] in the limit that the size of S/D contacts is the same as the NW diameter (Figure 2a). The simulations (Figure 2b) show that the electrostatic potential is close to the applied 1 V over a substantial portion of the channel. These results suggest that it should be possible

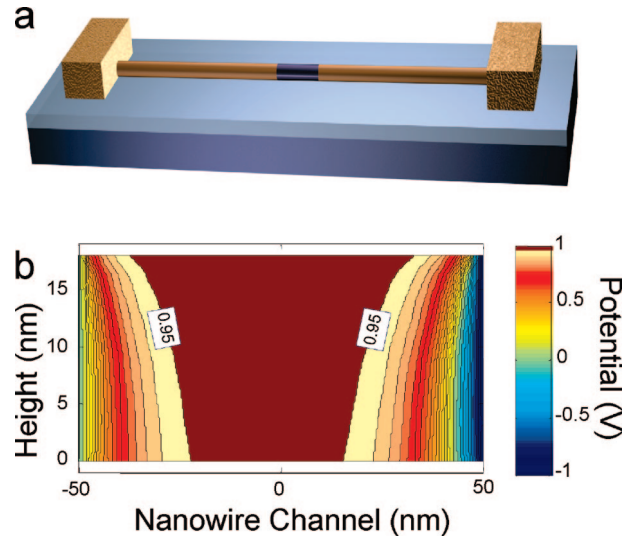

Figure 2. (a) Schematic of NW (dark blue) contacted with nanoscale electrodes (gold). (b) Plot of electrostatic potential distribution using conditions of Figure 1c, except that contact width and thickness are the same as the NW diameter.[15]

to achieve close to ideal gate coupling in the case where the S/D contacts are similar in size to the NWFET.

Previous studies have shown SiNWs can be transformed to silicide NWs[16,17] as well as partially converted to form metallic NiSi−Si−NiSi NW heterostructures by solid state reaction,[16,18] thus yielding electrode structures similar to Figure 2a. We have developed a similar approach for the Ge/Si core/shell NWs to form $NiGe_xSi_y$ NW contacts and subsequently deposit high-k HfO_2 dielectric and gate electrodes to complete the NWFETs, as illustrated in Figure 3a. To prepare the $NiGe_xSi_y$-Ge/Si-$NiGe_xSi_y$ axial heterostructures, we (i) fabricate a longer channel device (0.5 μm) by electron-beam lithography and then (ii) anneal the sample in consecutive steps, which leads to stepwise increases in the lengths of the $NiGe_xSi_y$ NW regions and concomitant reductions in the Ge/Si NW channel length.[19] The stepwise annealing process was used to enable sufficient control of channel length in the sub-100 nm regime. Before top-gate fabrication, the Ge/Si channels were characterized by SEM (Figure 3b). These images show a clear contrast along the NW, with bright sections emerging from the Ni contacts,

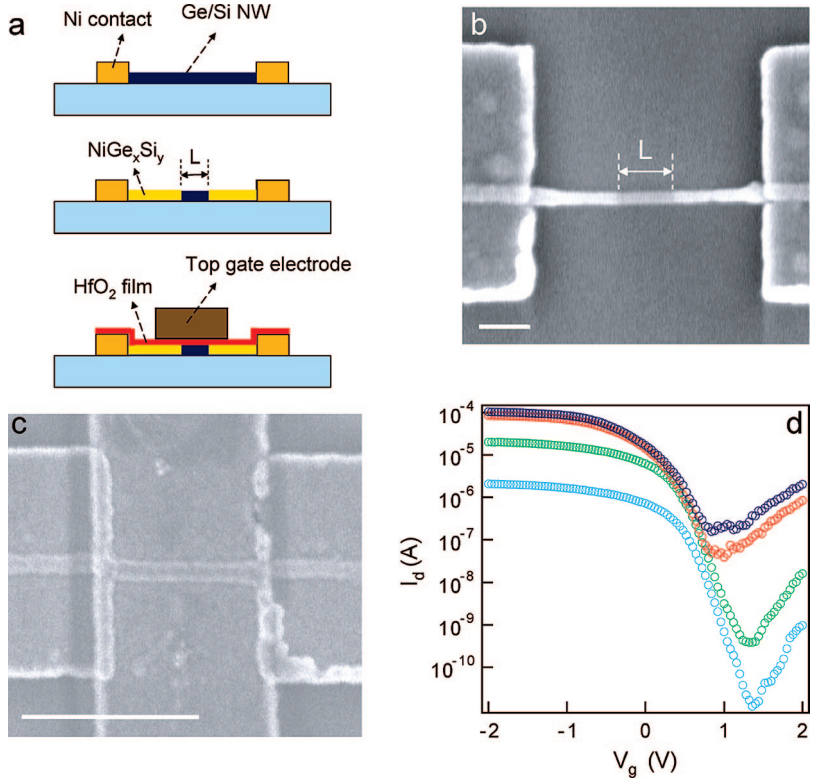

Figure 3. (a) Schematic of the fabrication process for sub-100 nm channel Ge/Si NWFETs with nanoscale NiGe$_x$Si$_y$ source/drain electrodes. (b) SEM image of a device before ALD deposition of HfO_2. Scale bar is 100 nm. (c) SEM image of top-gated NWFET. Scale bar is 500 nm. (d) Transport data from a 100 nm channel length device, with cyan, green, red, and dark blue data corresponding to $V_{ds} = -10$ mV and -0.1, -0.5, and -0.8 V, respectively.

which correspond to the metallic NiGe$_x$Si$_y$, and a dark segment sandwiched in between, which corresponds to the unreacted Ge/Si NW and taken as the effective channel length, L. The formation of metallic NiGe$_x$Si$_y$ during device annealing was further confirmed by two-probe transport studies of completely transformed NWs (see Supporting Information Figure S1). Finally, top-gate structure was completed as shown in Figure 3c.[13]

Typical performance of a 100 nm channel length device prepared in this manner with NiGe$_x$Si$_y$ NW S/D contacts is shown in Figure 3d. Significantly, the off-state current is reduced by a factor of 4000 for $V_{ds} = -10$ mV for the device with nanoscale electrodes compared to lithographically defined 100 nm channel length devices (Figure 1b). The subthreshold slope is also improved to 140 mV/decade and shows no bias voltage dependence. In contrast, the subthreshold slope was bias voltage dependent and increased to above 1000 mV/decade at higher biases for the lithographically defined 100 nm channel length devices. These comparisons demonstrate that deleterious electrostatic screening effects were suppressed by scaling the contact size.

We have used this approach to fabricate and study NWFETs with sub-100 nm channels and show representative output and transfer characteristics for devices with channel lengths of 70 and 40 nm in Figure 4. The family of I_d-V_{ds} curves shows that the drain current, I_d, first increases and then saturates with increasingly negative drain voltage. Analysis of the transfer data for the 70 nm device (Figure 4b) yields a maximum drain current I_d(max) of 121 μA at $V_g = -2$ V and a peak transconductance, $g_m = dI_d/dV_g$, of 78 μS at drain bias voltage $V_{ds} = -0.5$ V. Correspondingly, the data for the $L = 40$ nm device (Figure 4d) yields an I_d(max) of 152 μA and g_m of 91 μS. The observed increases in I_d(max) and g_m with decreasing channel length in these data is consistent with reduction in channel resistance as the device size is reduced.[10] We also note these I_d(max) and g_m are the best values obtained to date in single semiconductor NW or CNT FETs.[7,8a–f,10,20]

These new data can be compared in a robust manner to longer channel Ge/Si NWFETs[10] and state-of-the-art Si devices[21] by adopting the conventions used for planar devices.[22] First, the on and off current values are measured at $V_{g(on)} = V_T - 0.7V_{dd}$ and $V_{g(off)} = V_T + 0.3V_{dd}$, where V_{dd} is the power supply voltage and V_T is the threshold voltage. Second, the values are scaled to the device width,[10] where we use the total Ge core diameter D_{core} as the device width.[23] Comparison of the present data to longer channel Ge/Si NWFETs[10] shows improvements in scaled g_m and I_{on} for the 100 nm device (Table 1). The g_m values for 70 and 40 nm devices also exceed previous results for $L = 190$ nm (and 1 μm) devices, although I_{on} remains lower as a result of the fact that V_{dd} is 50% of the value used in earlier device measurements. In addition, the $L = 100$, 70, and 40 nm channel length devices exhibit values of the scaled I_{on} and g_m that exceed state-of-the-art Si p-MOSFETs by factors of 2–3 and 5, respectively, even though a much smaller V_{dd} of 0.5–0.8 V was used in our study, compared to $V_{dd} = 1.2$ V used in the MOSFET data. We attribute these latter perfor-

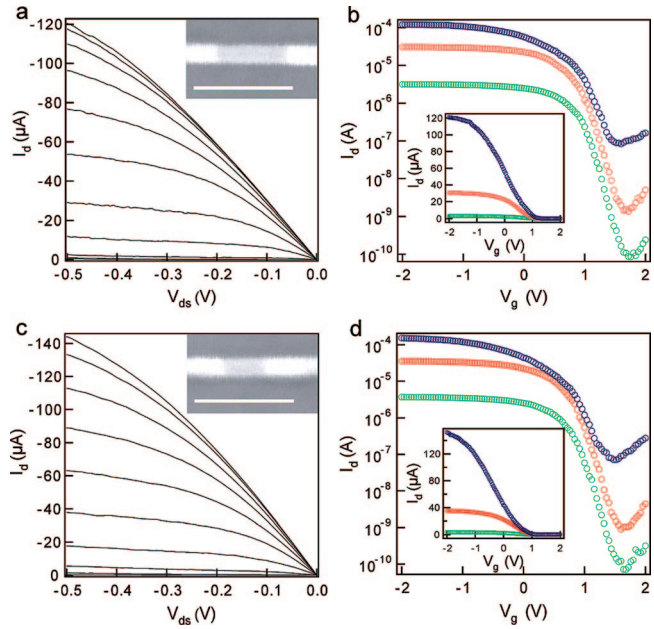

Figure 4. Transport characteristics of sub-100 nm channel length Ge/Si NWFETs. (a,c) I_d-V_{ds} data for $L = 70$ and 40 nm devices, respectively; V_g varies from −2 to 2 V in increments of 0.4 V from top to bottom. The insets show respective SEM images of the 70 and 40 nm devices; scale bars are 100 nm in both images. (b,d) I_d-V_g data for $L = 70$ and 40 nm devices, respectively. Insets show data on linear scale. The blue, red, and green data points correspond to $V_{ds} = -10$, −100, and −500 mV, respectively.

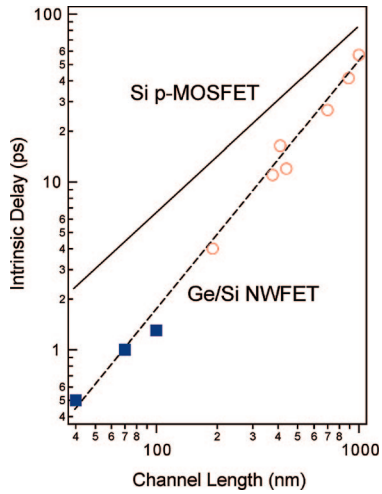

Figure 5. Length dependence of intrinsic delay is shown and compared with Si p-MOSFET results. Open circles represent data from ref 10. Solid squares are from this work. C was determined by numerical simulation[10] as $C_L = 800$ aF μm^{-1}.

mance improvements to a suppression of scattering in the clean quasi-one-dimensional Ge/Si NWs[24] and discuss this point further below.

Another important metric and point of comparison for FET performance is the intrinsic gate delay, $\tau = CV/I$, where C is the gate capacitance, $V = V_{dd}$, and I is on-current, I_{on}, as defined by the V_{dd} window criteria discussed above. The intrinsic delay can be considered as the time scale for depletion of transistor gate charge CV at the on-state and therefore is an indication of how fast a transistor operates.[3] A summary of the results from 10 Ge/Si NWFETs versus L and the corresponding scaling for Si MOSFETs (Figure 5) highlights several key points. First, the scaling of τ is more favorable for Ge/Si NWFETs than Si MOSFETs with a slope of ∼1.5 versus ∼1.1. Second, the data show clear speed advantage at a given L for the Ge/Si NWFETs. For example, 1 THz switching speed ($\tau = 1$ ps) is possible with $L < 70$ nm versus ∼30 nm for p-MOSFET.[22] Significantly, the 2 THz intrinsic speed indicated for the 40 nm device, represents the highest frequency among NWFETs and p-MOSFETs[22] and is comparable to the best value observed for CNT FETs.[7a,22] We note that it remains a challenge to verify such intrinsic behavior due to, for example, the effects of parasitic capacitance.

We have suggested that the excellent performance exhibited by the Ge/Si NWFETS can be attributed to a suppression of scattering in this quasi-one-dimensional system. One manner to evaluate this idea is to determine how close the NWFET operates to the scattering-free, ballistic limit.[25] We analyzed the performance of the $L = 70$ and 40 nm Ge/Si NWFETs using a semiclassical,

Table 1. Ge/Si NW and MOSFET Device Comparison

	Ge/Si NWFETs				p-Si MOSFET
	$L = 190$ nm[a] ($V_{dd} = 1$ V)	$L = 100$ nm[b] ($V_{dd} = 0.8$ V)	$L = 70$ nm[b] ($V_{dd} = 0.5$ V)	$L = 40$ nm[b] ($V_{dd} = 0.5$ V)	$L = 35$ nm[c] ($V_{dd} = 1.2$ V)
I_{on}/D_{core} (mA/μm)	2.5	3.3	1.8	2.1	1.06
g_m/D_{core} (mS/μm)	4.1	6.3	5.3	6.2	1.32

[a] Ref 10. [b] This work. [c] Ref 21.

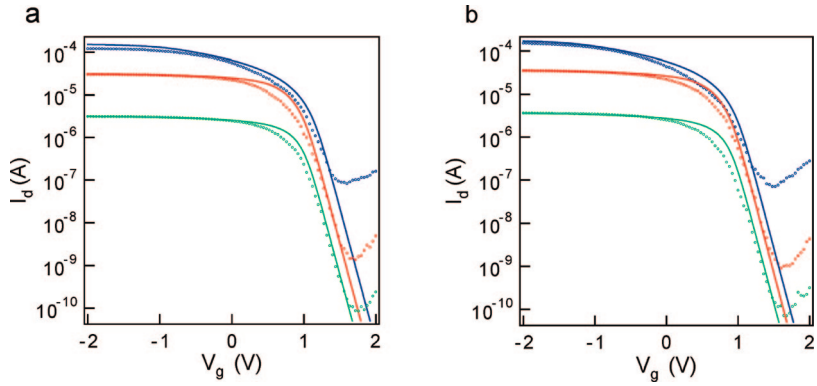

Figure 6. (a,b) Comparison of simulated and measured transfer characteristics for 70 and 40 nm Ge/Si NWFETs, respectively. Symbols are experimental data, and solid lines are ballistic simulations. Green, red, and blue data points correspond to $V_{ds} = -10$, -100, and -500 mV, respectively. The significant deviation between measurements and simulations in the off-state are due to the ambipolar conduction and tunneling effects not included in the simulation.

ballistic transport model[25,26] coupled with a $sp^3d^5s^*$ tight-binding model[27] to describe the electronic structure of Ge NW core.[12,28] Comparison of the calculated and experimental I_d-V_g transfer characteristics (Figure 6) shows very close agreement for low drain biases of $V_{ds} = -10$ and -100 mV, which suggest that the experimental devices deliver dc current close to the ballistic limit. At a higher bias of $V_{ds} = -0.5$ V, the simulation results deviate from the experimental measurements,[29] which indicate the importance of inelastic scattering process such as high-field induced optical phonon scattering.[30] An estimate of the potential importance of these deviations was made by comparing the ratio of experimental and simulated on-currents at $V_g = -2$ V and $V_{ds} = -0.5$ V, which yields a value of ca. 80% and 90% for 70 and 40 nm devices, respectively. Thus we conclude that the sub-100 nm Ge/Si NWFETs operate very close to the ballistic limit.

In summary, we have described the first studies of the size-dependent performance limits of Ge/Si NWFETs in the sub-100 nm channel length regime. Metallic $NiSi_xGe_y$ NW electrical contacts were used to define sub-100 nm Ge/Si channels by controlled solid-state conversion of Ge/Si NW. Electrical transport measurements and modeling studies demonstrate that the nanoscale metallic contacts overcome deleterious short-channel effects present in lithographically defined sub-100 nm channels. Electrical transport data acquired on 70 and 40 nm channel length Ge/Si NWFETs yielded scaled transconductances of 5.3 and 6.2 mS/μm and scaled on-currents of 1.8 and 2.1 mA/μm, which exceed significantly the best reported values for planar p-Si MOSFETs. In addition, analysis of the intrinsic switching delay shows that terahertz intrinsic operation speed is possible when channel length is reduced to 70 nm and that an intrinsic delay of 0.5 ps is achievable in our 40 nm device. Comparison of the experimental data with simulations based on a semiclassical, ballistic transport model suggests that these sub-100 nm Ge/Si NWFETs with integrated high-κ gate dielectric operate very near the ballistic limit. The near ballistic transport in the Ge/Si NW short channel devices may open the door to ultrafast nanoelectronics based on the bottom-up concept[4,31] and could extend the roadmap for high-performance logic.[1]

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Supporting Information Available: Two-probe current versus voltage curve for a 0.5 μm long $NiGe_xSi_y$ NW; current−voltage data recorded for a larger voltage range. This material is available free of charge via the Internet at http://pubs.acs.org.

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(13) Epitaxial Ge/Si core/shell NWs with average core diameter of 14.6 nm, Si shell thickness of 1.7 nm, and ⟨110⟩ core growth direction were prepared under the conditions described previously (ref 9, 10, 11a). Degenerately doped Si wafer with 600 nm thermal oxide was used as the substrate. Ni source/drain (S/D) contact electrodes (50 nm thickness) were defined by electron-beam lithography and thermal evaporation. Then the whole nanowire and contacts were covered by 4 nm HfO_2 using atomic layer deposition (ALD) process (ref 10). 35 cycles for HfO_2 deposition were used at 110 °C, with each cycle consisting of 1 s water vapor pulse, 5 s N_2 purge, 3 s precursor, and 5 s N_2 purge. Tetrakis(ethylmethylamino)hafnium [$H_f(N(CH_3)(C_2H_5))_4$] was used as precursor. A second step of electron-beam lithography was used to define the top gate, followed by thermal evaporation of Cr/Au (5/50 nm).

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(15) The simulation was carried out using the program COMSOL Multiphysics and was simplified to consider electrostatic potential for the off-state. All parameters were based on the actual device: NW consists of 14.6 nm Ge (dielectric constant $\kappa = 16$), and 1.7 nm Si ($\kappa = 11.7$); electrode width is 600 nm and height is 50 nm; top-gate dielectric was treated as 4 nm half-surrounding HfO_2 with $\kappa \sim 23$ (ref 10). Two-dimensional plots in Figures 1c and 2b show potential distributions in the Ge core and Si dielectric shell.

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(23) Alternatively, I_{on} and g_m values can be calculated by scaling the electrostatic gate width, $D_{core}*\pi/2$, which corresponds to the half circumference of the NW channel in our top-gate device geometry. The scaled values of g_m and I_{on} for the 70 nm device are 3.4 mS μm^{-1} and 1.2 mA μm^{-1}, and 4.0 mS μm^{-1} and 1.3 mA μm^{-1}, respectively, for the 40 nm device. These values still exceed those of the state-of-the-art p-Si MOSFET.

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(29) The deviation of the threshold voltage between the experimental data and simulation data at high V_g can be attributed to the scattering mechanism. The back scattering will help carriers to fill up the negative k states and reduces the number of occupied subbands. Note that the number of charges in the device is determinate by the V_g at the device on-state. Therefore, the threshold voltage would be larger in the ballistic simulation than the actual device. Similar deviation is also observed in simulations for carbon nanotube devices (ref 7e).

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